Investigation on Isolated Failure Mechanisms in Active Power Cycle Testing

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Abstract

In the last decades, considerable effort has been invested to predict the operational lifetime of classical IGBT power modules. Most of these investigations were based on end-of-life active power cycling tests. Two dominant failure modes were hereby identified: solder fatigue and Al wire bond failure. However, the lifetime models derived from these accelerated tests could not discriminate between these failure modes. Recently, more reliable interconnection technologies were developed, and both failure modes can now be studied independently. The experimental results presented in this paper show that the failure modes cannot be described within one common lifetime model, as both the dependence on the temperature swing ΔT_j and the influence of the absolute mean temperature T_{jm} differ significantly for both failures. As a consequence, the extrapolation of accelerated test results might lead to erroneous lifetime expectations.

1. Introduction

Power electronic modules are subjected to thermo-mechanical stress during operation due to temporal variation of power losses. The resulting lateral and vertical temperature gradients, in combination with the different coefficients of thermal expansion (*CTE*) of the materials, produce mechanical stress in the interconnection layers. This generates degradation of the interconnection interfaces and thus limits the lifetime of power modules in applications.

Ever since the early days of classical power electronic modules, active power cycling tests have been applied to investigate their lifetime. Typical junction temperature swings ΔT_j occurring in state-of-the-art power applications only exceed 40K occasionally. Nevertheless, power cycling tests have to be conducted at higher ΔT_j – such as 70K or even 110K – in order to provoke an end-of-life failure within a reasonable and practical test time. There is some uncertainty associated with the lifetime estimation resulting from the extrapolation of these accelerated tests. This incertitude increases when several failure modes can occur and different failure mechanisms can be dominant within the parameter range of interest.

In a classical power module, the interconnections on the topside of the power chip as well as on the bottom side are subjected to degradation, as reported in several publications. While solder fatigue is the common failure mode for the die attachment to the ceramic substrate, Al wire bond lift-off is typically observed for the top side chip interconnection.

Chip solder fatigue is driven by thermo-mechanical stress induced by the mechanical deformation of the joint, resulting from the mismatch in material parameters of the joining partners, in combination with the temperature gradients evolving within the layer stack during module operation. Depending on the power density in the chip, the geometry, the chip temperature, and the solder material, the degradation of the solder can start either from the edges or from the center of the chip [1].

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In contrast, wire bond lift-off is caused by recurring thermally induced deformation of the Al wire bond foot on top of the Si die. The huge *CTE* mismatch between the wire material and the silicon chip results in local stress in the bond foot, leading to crack formation and propagation along grain boundaries inside the Al wire during power cycling ([2] and [3]). The thinner the Si chip, the more important is the influence of underlying layers for the thermal expansion of the die's surface. As a consequence, Al wires have a higher lifetime on thinner Si chips as these can more easily follow the thermal expansion of the substrates [4]. Additional stress is generated in the bond stitch by the mechanical deformation of the layer system. Thus, the wire bond lifetime is also affected by the bond loop aspect ratio.

Although crack formation occurs in both failure modes, the divergent driving factors and different affected materials should lead to dissimilar dependencies on the test parameters in active power cycle testing – such as the temperature swing ΔT_j and the absolute temperature T_{jm}, as demonstrated in [5]. However, only very few studies address the impact of different failure mechanisms on the lifetime prediction [6].

The LESIT project [7] in the 1990s was the first comprehensive test program that investigated the end-of-life capability of power modules by subjecting what were at the time state-of-the-art modules from different manufactures to active power cycling tests. The evaluation of the experimental results revealed that the temperature swing ΔT_j alone is not sufficient to predict the module lifetime. As a result, an Arrhenius term that accounted for the impact of the absolute temperature range on the module lifetime, and which is typically described by a medium temperature T_{jm}, was introduced. Thus, the first general lifetime model for classical power modules was presented that described the lifetime of a module not only as a function of the temperature swing ΔT_j but also as a function of the medium junction temperature T_{jm}.

The CIPS2008 lifetime model [8] presented by Bayerer et al. in 2008, which was based on a statistical analysis of a significant number of power cycling tests, suggested taking even more parameters into account – such as the power pulse duration t_{on}, the wire bond diameter d_{bond}, the current density in the wire bond stitch, and the chip's voltage class.

Still, all these recent lifetime model approaches do not reflect the existence of different failure modes as discussed above. In the past few years, improved interconnection technologies have been developed, which allow a significant extension of the lifetime of the interconnections compared to the classical technologies. The Ag diffusion sinter technique, for instance, yields far more reliable joints than classical solder interfaces [9]. And the implementation of Al-clad Cu wire bonds can enhance the power cycling lifetime considerably, compared to the classical Al wire bond technique, as shown in [10]. Combining advanced technologies with classical interconnection techniques allows, for the first time, the investigation of the failure modes of wire bond degradation and solder fatigue independently. And in a second step, it enables their interaction to be studied.

The concept of separating failure modes was already introduced with an investigation into the impact of Al wire bond geometry on the power cycling lifetime [11]. The results demonstrated that the advantage of an optimized bond loop can only be fully utilized when solder fatigue is eliminated. Further studies focused on the impact of the medium temperature T_{jm} on the module lifetime [5] and showed that the dependence on this parameter is quite different for solder fatigue than it is for Al wire bond degradation.

To consider the impact of different failure modes correctly, a detailed failure analysis and investigations under different test conditions must be conducted when designing more accurate lifetime models. The investigation presented here concentrates on the impact of the temperature swing ΔT_j and medium junction temperature T_{jm}, with a focus on individual failure mechanisms.

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2. Isolating failure modes in active power cycle testing

2.1. Experimental setup

In order to isolate the failure mechanisms in active power cycling tests, two groups of modules were prepared. Group 1 consisted of commercial modules, namely the SKiM63 from Semikron, introduced in [9]. These modules have no base plate, the chips are sintered to the DBC, and the connection on the topside of the chip is realized by classical aluminum wire bonds with improved loop geometry. Due to the sinter joint between die and DBC, no solder fatigue is observed during power cycling, and only wire bond lift-off will occur. The modules of this group were bonded with an aspect ratio of *ar*=0.31. Group 2 consisted of modified modules of the same architecture, but with a more reliable topside contact in order to provoke solely solder fatigue. Thus, the chips were soldered with the standard process to the DBC, and aluminum-clad copper bonds [10] were implemented for the topside die connection.

The module itself consists of a six-pack configuration with three phase legs and has a nominal current rating of 300A. Each phase leg consists of an individual power DBC substrate and has separate terminals. For each switch, four 1200V-IGBT4 chips are connected in parallel (Fig. 1). The chip data are presented in Fig. 2.

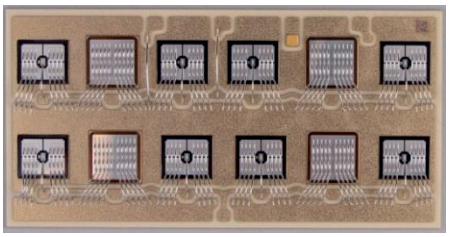

Fig. 1. Substrate of one phase leg of SKiM63

chip	IGBT4 1200V
area	9.12 x 7.71 mm²
thickness	120µm
I_{Cnom}	75 A

Fig. 2. Chip parameter

For each test run, one module of group 1 and one module of group 2 were mounted on identical water coolers. Both IGBT switches of one phase leg of each module were subjected to the load current, and the modules were connected in series, as shown in Fig. 3.

Two series of power cycling tests were performed on both groups. The tests of the first series are characterized by a constant minimum temperature T_{jmin}=const.=40°C, whereas the power cycling tests of the second series are characterized by a constant maximum temperature of T_{jmax}=const.=150°C. The temperature swing ΔT_j was adjusted to ΔT_j= 50K, 70K, 90K, 110K, and 130K, with resulting load currents I_{Load} ranging from 250A to 360A for a pulse duration of t_{on} =2s. The values of I_{Load}, t_{on}, and t_{off} remained constant during all power cycling tests. Thus, no compensation was provided for possible changes in ΔT_j or V_{CE} produced by degradation mechanisms. A 20% increase in the temperature swing ΔT_j or a 5% increase in the collector-emitter voltage drop V_{CE} were defined as common failure criteria. The test parameters of the two test series are summarized in Fig. 4. The results of a previous test series performed on the same groups of modules with different test parameters [5] was added for comparison and are included in the analysis below.

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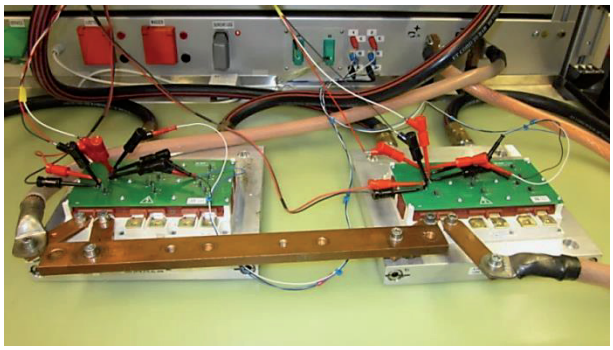

Fig. 3. Experimental test setup with two SKiM63 modules and one phase leg of each module connected in series

	This investigation		Previous results [5]
Load pulse duration t_{on}	2s		7s
Load current I_{Load}	250A - 360A		300A – 330A
Target conditions	Series 1	Series 2	
T_{jmin} [°C] / T_{jmax} [°C]		+100 / +150	-20 / +90
T_{jmin} [°C] / T_{jmax} [°C]	+40 / +110	+80 / +150	+10 / +120
T_{jmin} [°C] / T_{jmax} [°C]	+40 / +130	+60 / +150	+40 / +150
T_{jmin} [°C] / T_{jmax} [°C]	+40 / +150	+40 / +150	+65 / +175
T_{jmin} [°C] / T_{jmax} [°C]	+40 / +170	+20 / +150	

Fig. 4. Test conditions of test series

2.2. Power cycling test results for constant T_{jmin} or T_{jmax}

The experimental results of the conducted end-of-life power cycling tests are depicted in Fig. 5. The exact temperature swings show some minor deviations from the target conditions presented in Fig. 4 due to variations of device parameters of the individual DUTs.

To analyze the lifetime-determining factors of the different failure modes, a simple model was assumed, which reflects the impact of the medium temperature T_{jm} with an Arrhenius term and the temperature swing ΔT_j with a Coffin Manson factor. A general scaling factor A covers all other influences, which were either kept constant throughout the different tests or were not further investigated in the following analysis.

The resulting equation for the lifetime estimation is as follows:

$$n\left(\Delta T_j, T_{jm}\right) = A \cdot \Delta T_j^{-\alpha} \cdot \exp\left(\frac{E_a}{k_B \cdot T_{jm}}\right)$$

Least square fits were performed for group 1 (wire bond lift-off) and group 2 (solder fatigue) samples on the test results of both test series (constant T_{jmin}=40°C and constant T_{jmax}=150°C), also including the data presented in [5], in order to obtain the exponent α of the Coffin Manson factor and the activation energy E_a of the Arrhenius term in dependence of the failure mode. Since the load pulse duration data for series 1 and 2 (t_{on}=2s) differed from that from the previous results (t_{on}=7s) presented in [5], different scaling factors had to be assumed in the fit procedure.

The deduced parameters and the lifetime curve of the test series 1 samples tested at constant T_{jmin}=40°C are illustrated in Fig. 5. The comparison of the Coffin Manson exponents

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α_{Bond}=4.42 and α_{Solder}=3.5 reveals a higher dependency on the temperature swing ΔT_j for the bond reliability, while the solder fatigue is less affected by the temperature swing. Furthermore, solder fatigue is the lifetime limiting failure mechanism for low temperature swings ΔT_j. In the range around ΔT_j=100K, where accelerated tests are often conducted, both failure mechanisms are comparable in lifetime. Their interaction may even accelerate the end of life so that a lower number of cycles is actually expected for a classical module with both an aluminum bonding on the topside and a solder layer for the die attachment. However, this was not investigated experimentally.

For even higher temperature swings, the dominant failure mode changes to wire bond lift-off. An activation energy of $E_{a,bond}$=0.042eV and of $E_{a,solder}$=0.097eV was deduced for bond failure and solder fatigue, respectively. These values illustrate the very weak influence of the medium junction temperature T_{jm} on the wire bond lift-off and the higher impact on the solder fatigue mechanism. Therefore, the medium junction temperature T_{jm} only plays a minor role for power cycling lifetime of solder-free Al-wire-bonded sinter modules.

The difference relative to the temperature dependency can be explained by the physics of the failure mechanisms. During operation, the solder layer between chip and DBC is subjected to temperatures quite near the melting point of the solder. Thus, crack formation and propagation is enhanced as the temperature increases. In contrast, the bond interface undergoes comparable temperature levels as well, but the melting point of aluminum is far higher than the operating temperatures. On the other hand, crack formation in the interconnection between Si chip and Al bond is more sensitive to temperature swings due to the larger difference in the *CTE* of the involved materials.

A comparable behavior was observed for the power cycling test series 2, with a constant maximum temperature of T_{jmax}=150°C. The results are illustrated in Fig. 6. For low temperature swings ΔT_j, the solder fatigue is the prevalent failure mode in this case as well, whereas the bond lift-off is dominant in the range of higher temperature swings ΔT_j. In the range of ΔT_j=100K, both failure mechanisms exhibit a comparable lifetime. In the presence of both failure mechanisms, they could conceivably accelerate each other, so that a shorter lifetime than is presented in Fig. 6 might occur for classical modules.

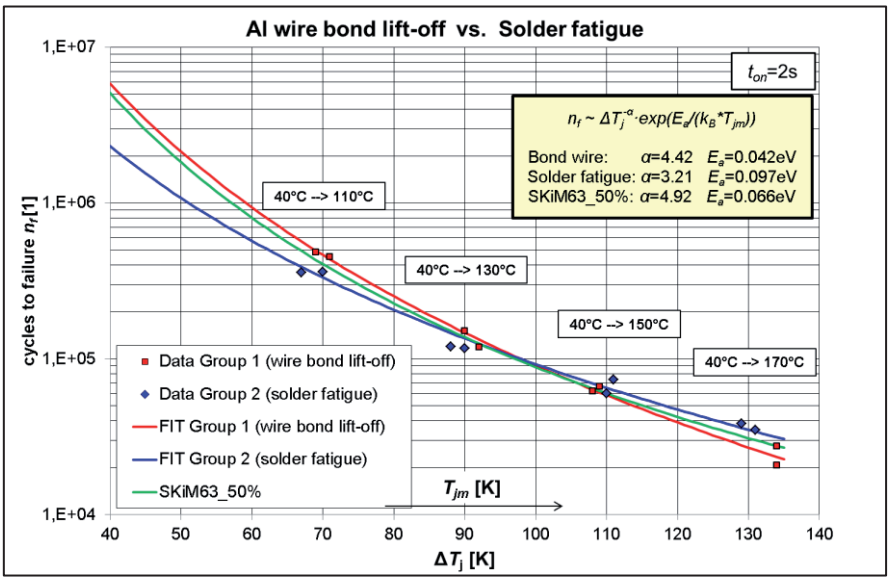

Fig. 5. Test series 1: Lifetime n_f as a function of temperature swing ΔT_j at a constant minimum temperature of T_{jmin}=40°C and comparison to the SKiM63 model [12]

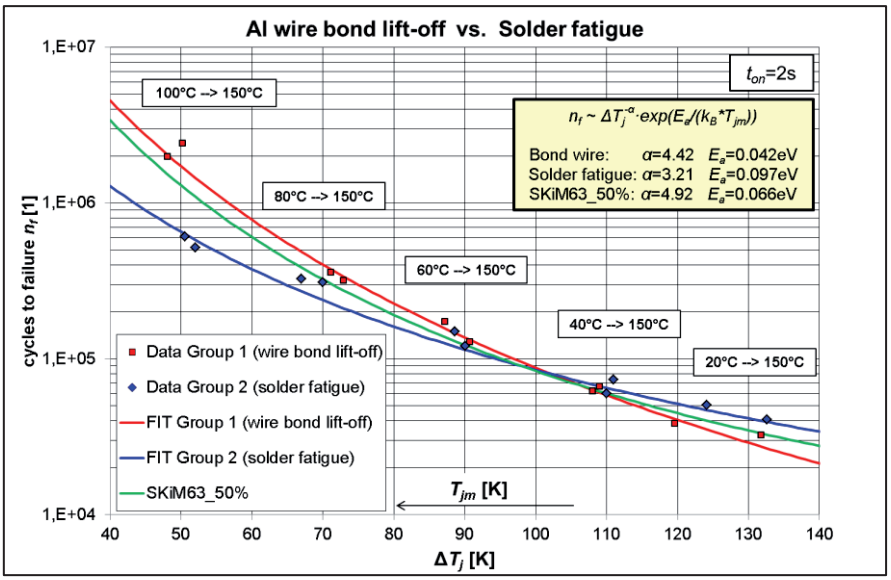

Fig. 6. Test series 2: Lifetime n_f as a function of temperature swing ΔT_j at a constant maximum temperature of T_{jmax}=150°C and comparison to the SKiM63 model [12]

2.3. Power cycling test results for a constant temperature swing ΔT_j=110K

The experimental results from a previous investigation with constant junction temperature swing ΔT_j=110K at different medium temperatures [5] were included in the database for the least square fits. In contrast to the new results shown in Fig. 5 and Fig. 6, these tests were conducted with a constant load pulse duration t_{on}=7s. As the influence of the load pulse duration on the power cycling lifetime of the solder layer is unknown, the fit procedures had to take into account a different scaling factor A^* for the data points of the previous investigation. The result of the fit procedure in comparison to the experimental data is depicted in Fig. 7.

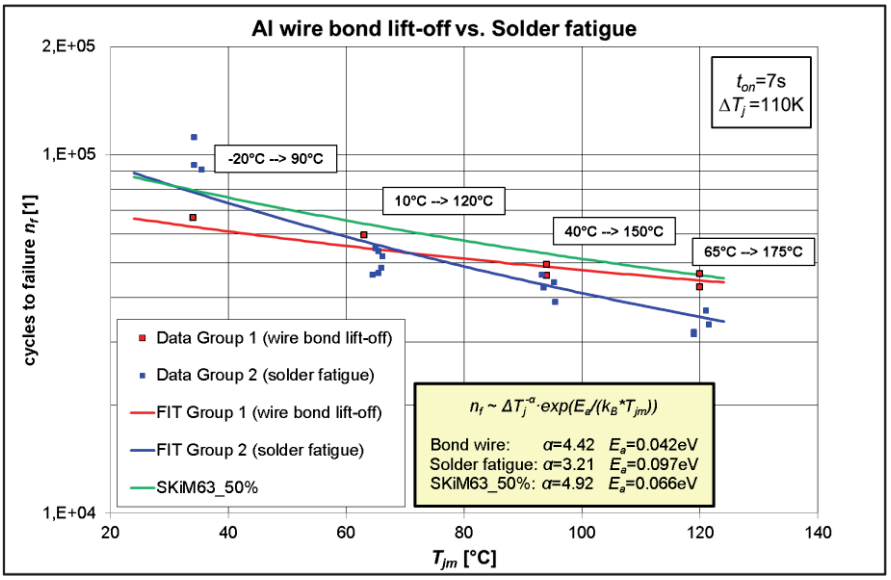

Fig. 7. Lifetime n_f as a function of temperature level ΔT_{jm} at a constant temperature swing of ΔT_j=110K and comparison to the SKiM63 model of [12]

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The fit, based on the data set derived from the actual and the previous investigation, confirms that the dependence on the medium temperature is much more pronounced for solder fatigue and less distinct for wire bond lift-off. For the individual test condition at constant temperature swing ΔT_j =110K, solder fatigue is the dominating failure mechanism in the range of high medium junction temperature, whereas wire bond lift-off prevails for low-medium junction temperature. The SKiM63 lifetime model [12] for a 50% survival probability predicts a higher lifetime for small medium temperature than the fit with the experimental data presented here. However, all experimental results are better than 80% of the SKiM63 lifetime prediction, which, from statistical assessment, predicts a survival probability of 85%.

The comparison of the test results for +40°C→+150°C in Fig. 7 with the test results for the same condition in Fig. 5 and Fig. 6 shows the impact of the different load pulse duration t_{on} in both test sequences. Increasing lifetime for decreasing t_{on} was already found in the SKiM63 model for wire bond lift-off [12] and is confirmed by the new results. The solder fatigue seems to exhibit an even stronger lifetime increase with decreasing pulse duration. However, the results for only two values of pulse duration are not sufficient to derive a general dependency of solder fatigue mechanisms on load pulse duration t_{on}.

2.4. Evaluation of results

Some general aspects can now be derived from the presented test results: Solder fatigue exhibits a stronger dependence on the medium temperature and a weaker dependence on the temperature swing than Al wire bond failures do. All other details of the presented results, such as intersection points of the two lifetime curves, are closely related to the investigated test structures and the applied test conditions.

The tested devices were power modules without base plate. Thus, any impact of solder fatigue in the solder joint between the substrate and a base plate was eliminated. When transferring these results to base plate modules, the additional limitation of the base plate interface must be taken into account. Furthermore, the same surface metallization on the DBC substrates was used for both the Ag-diffusion-sintered and the soldered-chip specimen. The NiAu surface could have an impact on solder degradation as was recently reported [13]. Additionally, the solder material and process might influence the solder fatigue lifetime. Finally, the IGBT chip dimensions (size and thickness) could also affect the solder fatigue process. The wire bond geometry also influences the wire bond lifetime, as investigated in [12].

The test conditions applied also affect the details of the correlation between solder fatigue and wire bond lift-off. For the same temperature swing and medium temperature, test results could be quite different when performed at different load pulse durations, giving different positions of intersection on the temperature swing scale.

3. Conclusion

In active power cycling tests on classical power modules, two dominant failure mechanisms are known and well-described in literature: Al wire bond lift-off and solder fatigue between the chips and the substrate. A third failure mechanism is the fatigue in the system solder layer between the base plate and the substrate, which becomes dominant only for long load pulse duration, but which might contribute to the degradation process at medium pulse length.

The majority of existing lifetime models do not differentiate between different failure modes. These models try to characterize all failure modes by a single set of parameters due to the fact that advanced technologies for separating these failure modes were not available. The progress in interconnection technology has changed this situation. Advanced module designs are available, which eliminate the base plate and thus also the potential solder fatigue between base plate and substrate. Ag diffusion sintering is established as a more reliable replacement for the classical solder interface, and Al-clad Cu wires exhibit a superior

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lifetime compared to classical Al wire bonds. The combination of these technologies allows, for the first time to confine the degradation in active power cycling to a single failure mode. This also means that the lifetime-determining factors can be investigated separately, without interaction.

The presented experimental results of active power cycling tests on two groups of specimens under identical cycling conditions enables the impact of the temperature swing and the medium junction temperature to be determined separately for each failure mode. Solder fatigue shows a smaller dependency on the temperature swing, but a stronger impact of the medium junction temperature than Al wire bond lift-off. The results for the Al wire bond lifetime correspond well with a lifetime model derived from a more extensive investigation presented previously [12].

The results for the solder fatigue should be regarded as initial results about the dependency on temperature swing and medium junction temperature. More tests are necessary to determine all other influencing factors, with the goal of deriving a general model for solder fatigue lifetime.

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