

# Application Note AN 19-001

Revision:	00
Issue date:	2019-05-29
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Keyword: NPC, TNPC, IGBT, Driver, 3-Level

## Gate Driver Configuration and Short Circuit Protection for 3-Level Topologies

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### 1. General

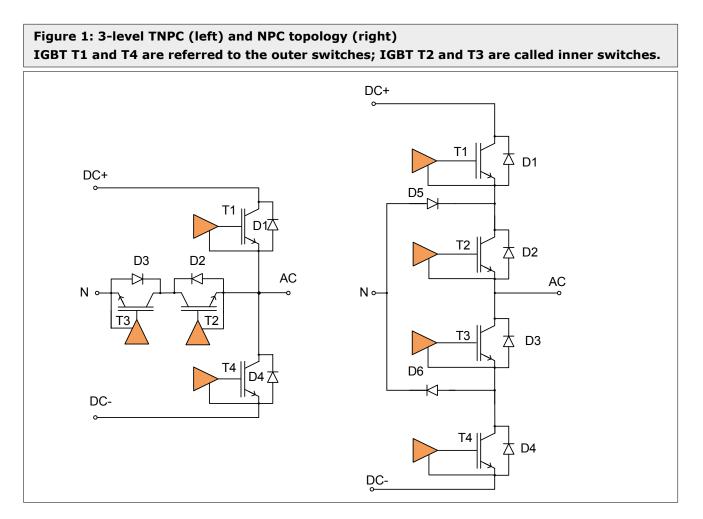
3-level topologies are mainly used in UPS and solar applications due to their high efficiency and low harmonic distortion of the grid. This application note describes the control and protection of power semiconductors in 3-level NPC and TNPC topologies. In this context the term IGBT is synonymous with power semiconductors. Essential for the design of the driver is to limit the voltage at the IGBT and handling of short circuits. This application note is structured accordingly.

After this introduction, chapters 2 and 3 explain the structure and switching pattern of the 3-level topology. Chapter 4 describes the commutation circuits and how to limit the voltage at the IGBT. Chapters 5 and 6 deal with the different short circuit scenarios and the design of the short circuit protection. The last chapter deals with special features of a short circuit detection. It is recommended to read the application note "3L NPC & TNPC Topology" [3] first.

#### 2. 3-Level Topology

The most common 3-level topologies are NPC and TNPC. Both topologies have four IGBTs per phase and therefore require four driver stages for control.



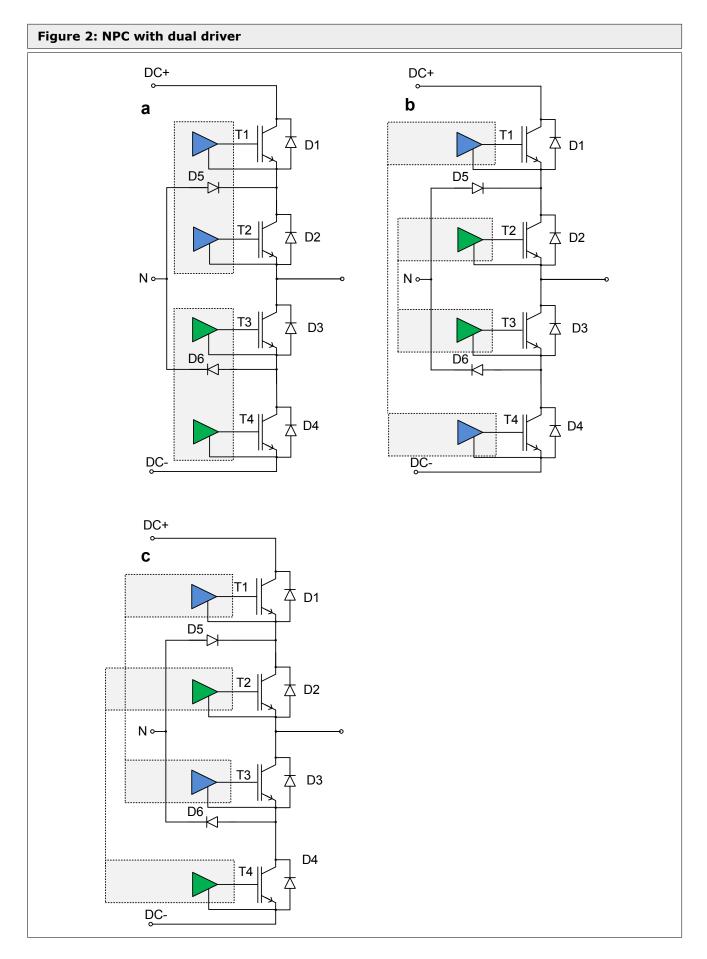


The driver stages can be designed with single drivers but also with commercially available dual drivers. The SEMIKRON SKYPER42LJ and SKYPER12 driver platforms are particularly suitable for 3-level applications due to their adjustable response to a short circuit detection. Figure 2 shows the possible connections of dual drivers to an NPC phase leg. This applies also to the TNPC topology because both topologies make use of the same pulse pattern. Referring to Fig. 2 the following variants exist.

- a) Driver 1 on IGBT T1 and T2. Driver 2 on IGBT T3 and T4.
- b) Driver 1 on the outer IGBTs and driver 2 on the inner IGBTs.
- c) Driver 1 on T1 and T3 and driver 2 on T2 and T4.

With variant a and b it must be possible to turn off the interlock function of the driver, because both IGBTs may be switched on at the same time. This application note discusses examples for both variants. With the 3-level topology, IGBT T1 and T3 are switched inverted with an interlock delay time between the switching states. Therefore, a standard half-bridge driver with interlock and dead time function can be used for variant c. The dead time does then not need to be generated by the controller. The same applies to IGBT T2 and T4.



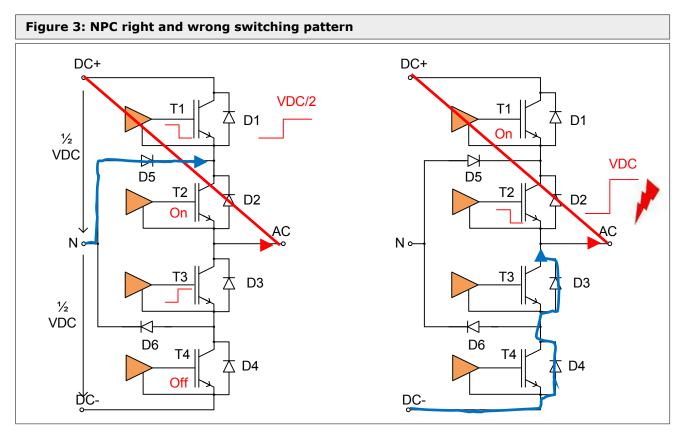




#### 3. Switching Pattern of a 3-Level Converter

#### 3.1 NPC topology

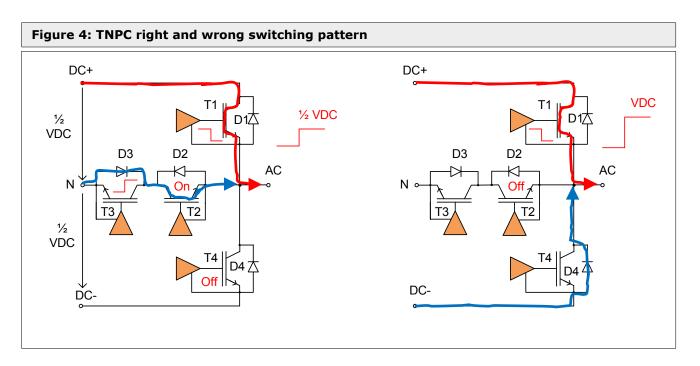
To protect the IGBTs from excessive voltage, the external IGBTs must be switched off prior to the internal IGBTs. The current commutates to diode D5 or D6, limiting the voltage at the IGBT to half the DC-bus voltage ( $1/2 V_{DC}$ ). The commutation is shown in Figure 3 for a positive current. This behaves analogously with a negative current. However, if IGBT T2 is switched off whilst IGBT T1 is switched on, the current commutates to the diodes D3 and D4. The full voltage V<sub>DC</sub> is then applied to T2. If the V<sub>DC</sub> is higher than the blocking voltage of the IGBT, it will be destroyed.



#### **3.2 TNPC topology**

As with NPC, in the TNPC configuration the outer IGBTs should be switched off prior to the inner IGBTs. As shown in Figure 4, the current commutates from T1 to D3 and T2. If, however, T2 is switched off prior to T1, the current commutates to D4 and not to the horizontal branch D3, T2. The commutation is then like a 2-level circuit. The peak voltage is higher because the commutation circuit is larger and the full DC-bus voltage is applied.





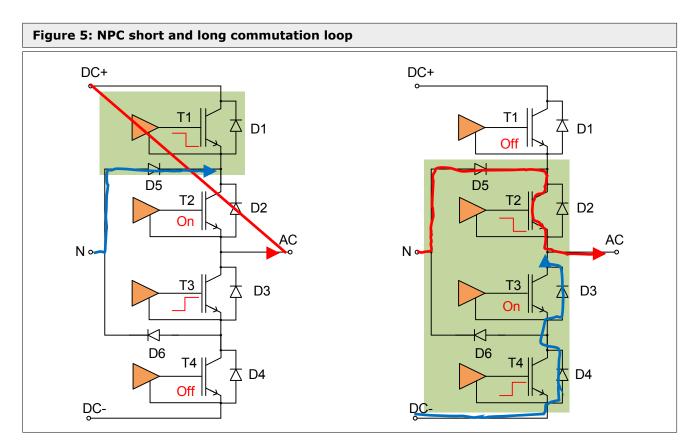
#### 4. IGBT peak voltage

#### 4.1 NPC topology

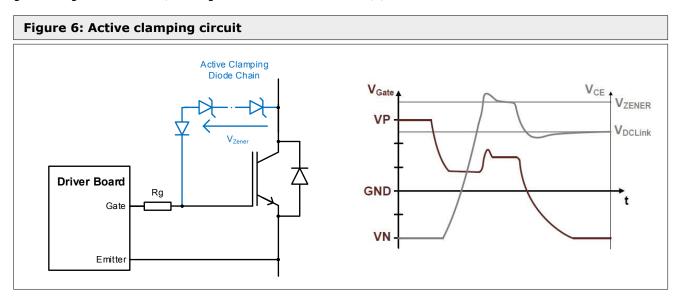
The NPC topology has two different commutation circuits, the short and the long commutation circuit. Figure 5 shows the commutation circuits for a positive current. The commutation loop is symbolized by the green rectangle. With active power ( $I_{out}$ >0 and  $V_{out}$ >0) the commutation takes place in the small commutation circuit, and with reactive power ( $I_{out}$ >0,  $V_{out}$ <0) in the large commutation circuit. The leakage inductances and thus the peak voltage during switching are higher with the large commutation circuit than with the small one. To limit the peak voltage, the gate resistors can be adapted or the voltage can be limited via a so-called "active clamping" circuit. When limiting with the gate resistors, it should be noted that in modern IGBTs the switch-off process can

only be controlled to a limited extent via the gate resistor [4].





In the active clamping circuit, diodes with Zener characteristics are connected from the collector to the gate. The voltage level where the clamping starts is set by the breakdown voltage of the diode chain. If, during a switch off, the  $V_{ce}$  rises beyond the  $V_{Zener}$  the clamping diodes become conductive. This current switches the gate on again until the  $V_{CE}$  voltage is reduced below the  $V_{Zener}$  reference.



#### 4.2 TNPC topology

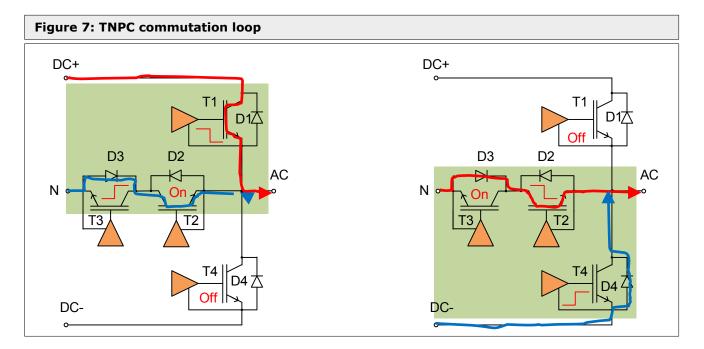
In TNPC topology, the inner IGBTs and the outer IGBTs have the same commutation circuit. The blocking voltage of the horizontal IGBTs (T2, T3) is often lower than the vertical IGBTs (T1, T4).

Example: Maximum DC-link voltage = 1000V. T1/T4 = 1200V IGBT/diode. Margin 1200V-1000V = 200V.

 $T_2/T_3 = 650V IGBT/diode. Margin 650V-500V = 150V.$ 

In this case voltage limiting measures like active clamping are often necessary for the horizontal IGBTs.





#### 5. Short Circuit Scenarios

The following deals with different short circuit scenarios.

- Short circuit outside the system beyond the device terminals (Figure 8). It is assumed that the inverter features current measurement and an AC side choke in each phase leg.
- Short circuit within the system in front of the choke (Figure 9). The current is not measurable by the current sensor and is not limited by the AC side choke. This is a fault in the system; for example an insulation defect or metal parts in the system.

In both cases, a distinction is made between a short circuit of

- phase to phase or
- phase to the DC-link.

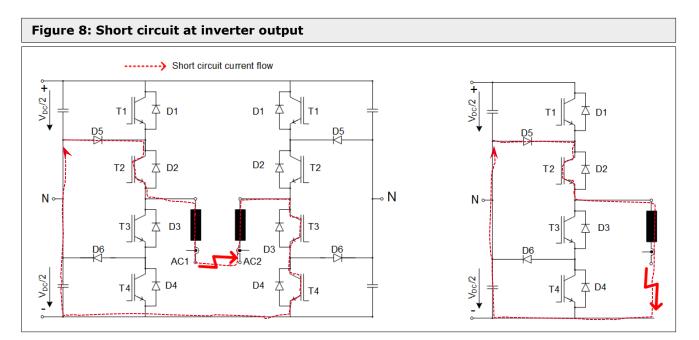
To explain the short circuit phase to phase, only two phases of the inverter are shown and for a short circuit phase to DC-link only one phase. The illustrations show the NPC variant, but the considerations also apply to the TNPC.

#### 5.1 Short circuit at the inverter output

The current sensor is in the short circuit path. When an overcurrent threshold is reached, the IGBTs are switched off in a specified sequence: first the outer IGBTs and then the inner IGBTs. The IGBTs should be switched off before the IGBT desaturates. This requires both fast current acquisition and an evaluation circuit. A positive effect is that the current rise is limited by the AC-choke. If only looking at this type of short circuit, no short circuit detection is necessary for the IGBTs. However, if the current still rises until the IGBT is desaturated, perhaps because the current detection is too slow, then this case must be considered as described in 5.2.

The desaturation of the IGBT usually occurs at 3-8 times of the nominal current, which may lead to the destruction of the IGBT. See [2] section 5.7.2. for a more detailed explanation of the desaturation behaviour. For an explanation of the "Dynamic short circuit protection", see the technical explanation of the driver board [5] and [6].

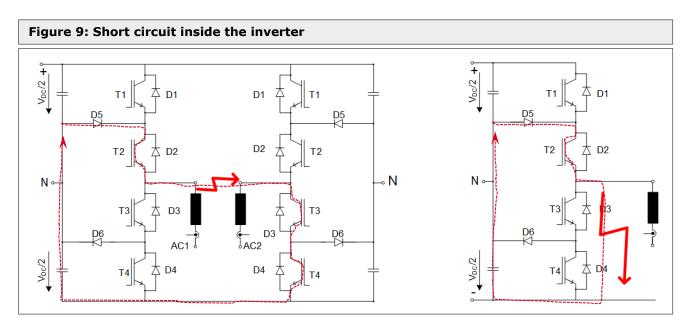




#### 5.2 Short circuit inside the inverter

The short circuit current is not detected by the current sensor. The current rises until the IGBT desaturates. The desaturation of the IGBT is detected by the dynamic short circuit protection of the driver. If the short circuit occurs close to the module, the current may rise at several kA/ $\mu$ s. This operation is only permitted if a short circuit time (t<sub>psc</sub>) with short circuit conditions is specified in the IGBT datasheet.

As shown in Figure 9, the current always flows through one of the outer IGBTs during a short circuit from phase to phase. If only inner IGBTs were involved, no short circuit current would flow because only the N-potentials are connected. With a short circuit phase to DC it is possible that only one inner IGBT is involved.



Another scenario of short circuit is the simultaneous switch-on of several IGBTs (e.g. T2, T3 and T4) due to incorrect control. If the DC voltage is higher than the blocking voltage of the IGBT, the IGBT that is turned on last (e.g. T1) will be destroyed by overvoltage if no active clamping limits the voltage.



#### 6. Short circuit protection design

In the event of a short circuit at the inverter output, overcurrent detection with a current sensor in each phase is sufficient, as shown in 5.1. In the following sections only the more severe internal short circuit of the inverter is considered.

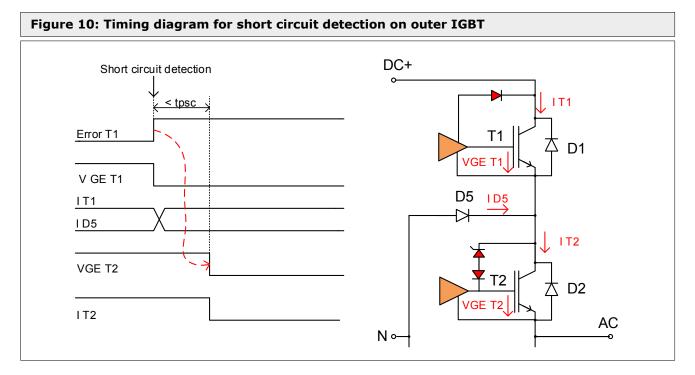
#### 6.1 Phase to phase short circuit protection

As the short circuit current always flows via one of the outer IGBTs, short circuit detection on these IGBTs is sufficient. In the event of a short circuit detection, the IGBT is immediately turned off via a soft-off resistor that is many times higher than the normal gate resistor. This allows the voltage at the IGBT to be limited to permissible values. The current commutates from the external IGBTs to the diodes D5 or D6. The error signal generated by the driver is fed to the controller on the user side, which in turn must switch off the inner switch within  $t_{psc}$ . To protect the inner switches from too high voltage when turned off with the standard  $R_g$  an active clamping circuit may be necessary.

In order to maintain this switch-off sequence, the inner IGBT must not switch off immediately if a short circuit is detected at the outer IGBTs, but only when the current from the IGBT has commutated to diode D5 or D6. This has to be considered when selecting the drivers and the error/fault handling. Figure 10 shows the timing diagram for a positive current.

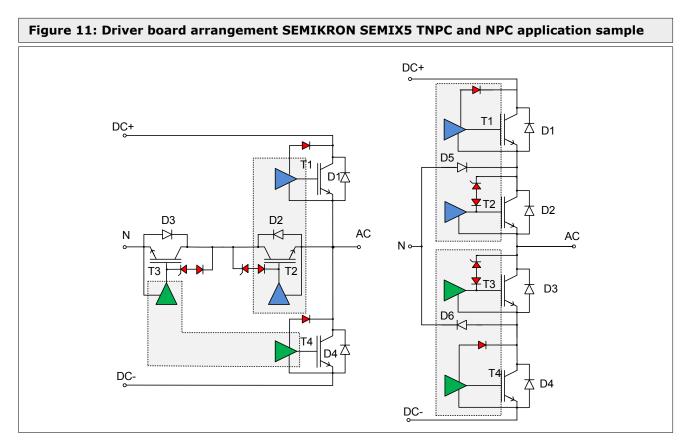
The conditions for TNPC are analogous. T1 detects the short circuit and turns off softly. The current commutates to D3 and T2. T2 is then switched off hard at high current.

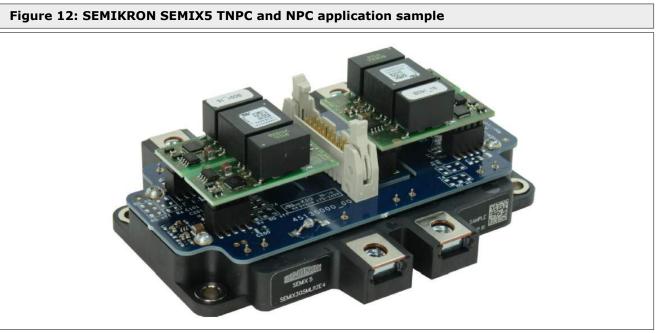
For an explanation of soft-off resistors please see the technical explanation of the driver board [5] and [6].



This protection is implemented in the SEMIKRON SEMIX5 TNPC and NPC application sample. Two SKYPER12 are used, one for T1, T2 and the other for T3, T4. Both drivers are operating in NPC mode. This means that the driver switches off on error but not the second stage of the driver board.







See [7] "TE - SEMiX5 1200V MLI SKYPER12 Driver Board" and [8] "TE - SEMiX5 TMLI SKYPER12 Driver Board"

#### 6.2 Phase to phase and phase to DC short circuit protection

Short circuit detection for the outer and inner IGBTs must be implemented for this purpose. In this case both phase-phase, phase-DC and phase-ground short circuits can be switched off.

If a short circuit is detected by the outer IGBTs, the shutdown is performed as described in section 6.1.

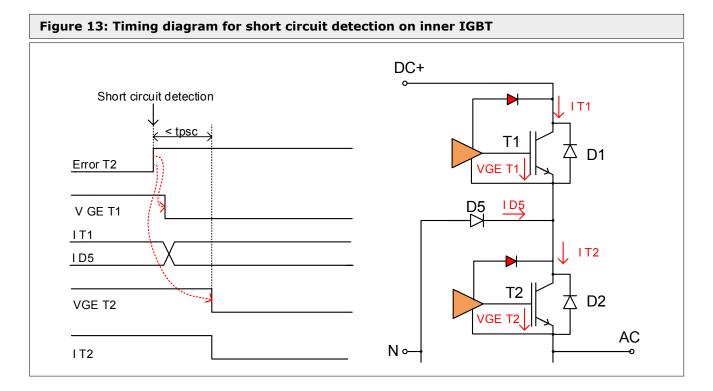


If a short circuit is detected by the inner IGBTs, these IGBTs do not switch off. The driver generates an error message. The controller on the user side then turns off the outer IGBTs if they were switched on. Once the current from the IGBT has commutated to the diodes D5/D6, the inner IGBTs are switched off. The switch-off sequence has to be managed by the control board. This short circuit switch off must occur within  $t_{psc}$ . The outer switches are turned off with the standard  $R_{goff}$ . Figure 13 shows the timing diagram for a positive current.

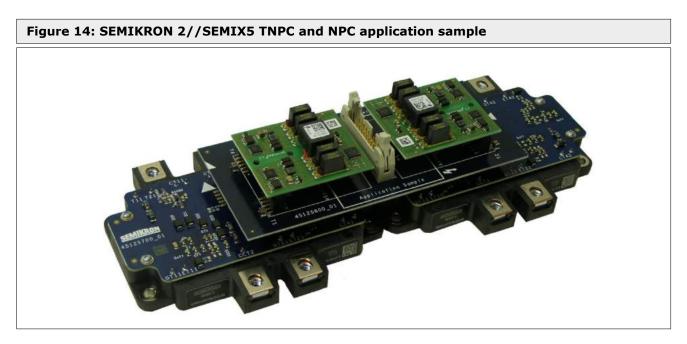
This switch-off sequence can be guaranteed with the SKYPER42LJ driver in the NPC module. In this mode, the IGBTs are not switched off when a short circuit is detected, but only an error is transmitted. Due to this stored error, the IGBTs are switched off with the soft-off resistor at the next regular switch-off pulse and can thus be protected against overvoltage.

This protection is implemented in the 2//SEMIX5 TNPC and NPC application sample. Two SEMIX5 modules are connected in parallel for an output power of approx. 250kW. Two SKYPER42LJ are used. The driver can be set to 2-level or MLI mode via a pin. The MLI application sample needs no active clamping diodes due to sufficient voltage margin while the TMLI offers active clamping diodes on inner IGBTs.

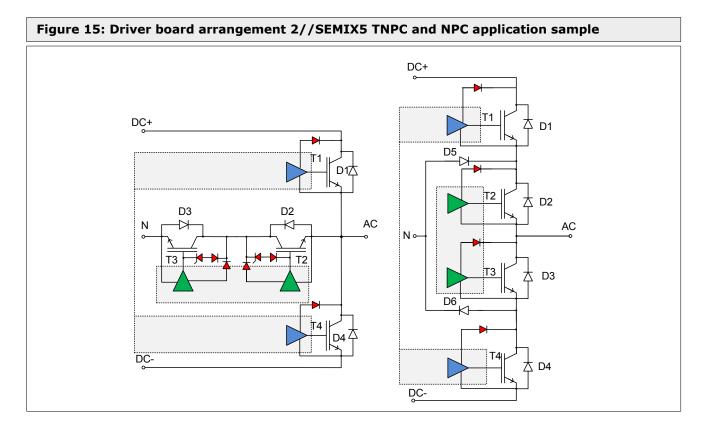
The driver for the inner IGBTs is operated in NPC mode and the outer IGBTs in 2-level mode. In a short circuit situation the IGBT turns off via the soft-off resistor.





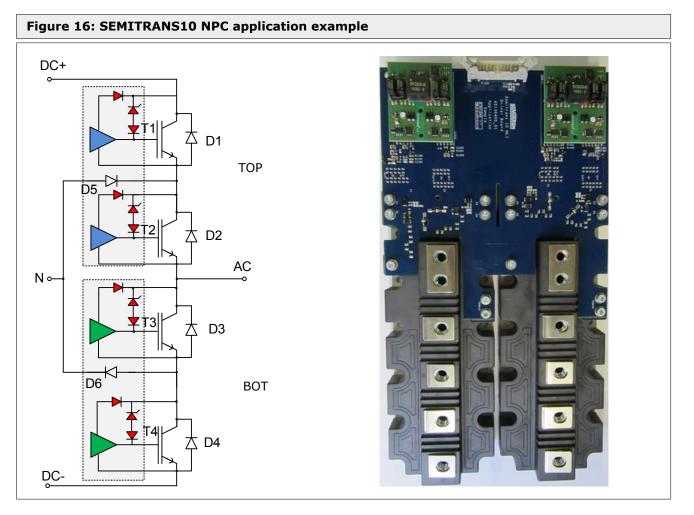


See [9] "TE - SEMiX5 1200V TMLI Parallel Driver Kit" and [10] "TE - SEMiX5 1200V MLI Parallel Driver Kit".





The best protection is guaranteed if all IGBTs have short circuit detection and active-clamping voltage limiting. In this case, each IGBT can be switched off immediately in the event of a short circuit without having to pay attention to a particular switching sequence. In case of an error message of one IGBT, all others are switched off immediately. 2-level drivers may be used. The disadvantage of this circuit is the high number of Zener diodes which increase cost and require space on the driver PCB. This protection is implemented in the SEMITRANS 10 NPC application sample.



See [11] "TE - ST10 MLI Driver Board - 11.04.2019\_rev04.pdf".

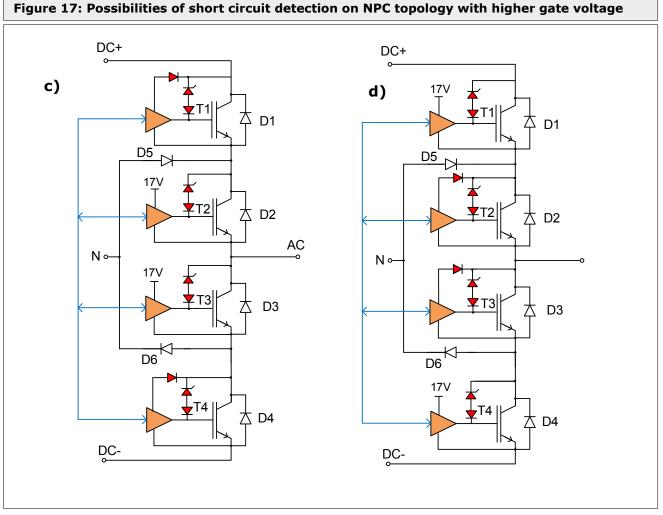


#### 7. Special Driver Board Setup for 3-Level

Short circuit detection and short circuit turn-off is more difficult with the NPC than with the TNPC. With the TNPC only one IGBT is in current conduction mode at the time of a short circuit, whereas with the NPC two IGBTs connected in series can be energised. When using IGBTs of the same type, both IGBTs may desaturate at the same time. This condition is undesirable because the IGBTs in desaturated condition have a high gain (large current change with small gate voltage change) and therefore tend to oscillate, which can result in destruction. The following describes options to prevent this.

- a. The case of desaturation is excluded by only allowing short circuits at inverter output . As described in 5.1.
- b. All four IGBTs feature active clamping and short circuit detection. If a short circuit is detected, the IGBT is switched off immediately. As described in 0, Figure 16.
- c. All four IGBTs feature active Clamping and the short circuit detection exists only for the outer switches. See Figure 17c. In addition, the **inner** IGBTs are supplied with a higher gate voltage than the outer IGBTs (e.g. with 17V). This is to ensure that the outer IGBTs always desaturate first. A disadvantage is that with an AC to DC short circuit, in which the outer switch is not involved, the short circuit current for the inner IGBTs becomes very high due to the higher gate voltage. The IGBT must then be switched off earlier than the specified short circuit time t<sub>psc</sub> in order not to be thermally destroyed.
- d. All four IGBTs feature active clamping, yet a short circuit detection only exists for the inner switches. See Figure 17d. In addition, the **outer** IGBTs are supplied with a higher gate voltage than the inner IGBTs (e.g. with 17V). This is to ensure that the inner IGBTs always desaturate first. Hence, all short circuit cases can be detected. If a short circuit is detected, the IGBT is turned off immediately and an error message is generated. The outer IGBTs are then turned off immediately. The Active Clamping circuit protects the IGBT from overvoltage, even if the inner IGBT turns off before the outer one.

Sometimes different  $V_{CE}$  short circuit detection levels and blanking times for inner and outer IGBTs are implemented to ensure the switch-off sequence. In practice, this measure usually does not work because component tolerances have a greater effect than the adjustable difference in  $V_{CE}$  detection level and blanking times.



#### Figure 17: Possibilities of short circuit detection on NPC topology with higher gate voltage

#### 8. Summary

Driver board configuration for peak voltage limitation and short circuit (SC) protection for both NPC and TNPC topology has been explained. For both outer IGBTs shall switch off prior to the inner IGBTs to limit the peak voltage.

Beside SC consideration, a peak voltage limitation by active clamping on the inner IGBTs may be necessary for TNPC circuit due to lower voltage margin and for NPC circuit because of higher inductance in the long commutation loop.

The SC in TNPC topology is easier to handle since only one IGBT is conducting. NPC topology is more difficult to handle since two IGBTs are connected in series, which could lead to simultaneous desaturation of both devices.

With desaturation detection only on outer IGBTs the SC between phases are detected but not from phase to ground. However, this solution is attractive since the effort and component count is relative low and the 3-level safe turn off sequence is guaranteed. Active clamping on inner IGBT may still be necessarv.

For SC protection to ground and between phases a desaturation detection on all IGBT has to be implemented. With different gate voltage on inner and outer IGBT of the NPC circuit the desaturation detection only on two IGBT is sufficient because the desaturation sequence is defined.

With active clamping diodes on all IGBTs the IGBT can be turned off immediately when the SC is detected. The advantage is that no switch-off regime has to be implemented and standard 2-level drivers can be used. However, high number of components especially Zener diodes are needed which



reduces the reliability of the system. Further, the design of active clamping is challenging because of diode tolerances.

If the SC current is detected by an AC side current sensor before the IGBT desaturases no desaturation detection on IGBT is needed. That is usually the case if the current slope is limited by an AC side choke. This reduces the driver effort significantly with the drawback of no short circuit robustness before the AC choke, e.g. due to isolation defects or wrong assembly in manufacturing.

It is up to the system designer to decide which protection level is sufficient for the application.



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#### Symbols and Terms

Letter Symbol	Term
DC+, DC-, N, AC	IGBT module power connection
G, E	IGBT module gate, emitter connection
V <sub>DC</sub>	DC-link voltage
V <sub>CE</sub>	IGBT collector-emitter voltage
V <sub>GE</sub>	IGBT gate-emitter voltage
R <sub>g</sub>	Driver board gate resistor
V <sub>Zener</sub>	Trigger voltage of Zener diode
V <sub>P</sub>	Positive gate voltage
V <sub>N</sub>	Negative gate voltage
t <sub>psc</sub>	Maximum time for short circuit duration
PE	Protective Earth
Error T1, Error T2	Error signal from IGBT T1 driver stage, IGBT T2 driver stage
I <sub>T1</sub> , I <sub>T2</sub> , I <sub>D5</sub>	Current of IGBT T1, T2 and Diode D5
ТОР	Top stage
ВОТ	Bottom stage
NPC Inverter	Neutral Point Clamped Inverter
MLI	Multi Level Inverter (same than NPC inverter)
TNPC Inverter	T-type of Neutral Point Clamped Inverter
TMLI	T-type of Multi Level Inverter (same than TNPC inverter)

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2]

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