High Current, Low Voltage Solution For Microprocessor Applications from 48V Input

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Abstract

A novel approach for providing microprocessor power directly from 48V is proposed. This solution enables high voltage, low current to be distributed throughout a system, minimizing distribution losses, while providing low voltage, high current direct from the 48V input in the most efficient manner possible. This solution is also extremely small, minimizing the required footprint at the microprocessor core, and extremely fast, eliminating the need for capacitors at the point of load.

1.0 Background

Evolving CMOS technology has been continuing to drive the core voltage of microprocessors down and the core currents of microprocessors up [1]. As the core voltage decreases and the current increases, the challenges for providing this power have been steadily mounting. Higher current results in exponentially higher dissipative losses both in synchronous MOSFETs and in copper distribution paths. Lower output voltages make the following equation impractical:

$$V_{OUT} = V_{IN} \cdot D \qquad \text{[Eq. 1]}$$

V_{OUT} is the Output (Microprocessor Core) voltage, VIN is the Input (Source) voltage and D is the duty cycle. In response to a smaller value of VOUT, D must also become smaller. This impacts the ratio of switching and core losses to dissipative losses in MOSFETs and magnetics. A lower source voltage could be considered to enable D to remain constant, however overall system efficiency would be impacted by the following relationship:

$$P_{LOSS} = I_{in}^{2} \cdot R_{S\_dist} \qquad \text{[Eq. 2]}$$

where P_{LOSS} is the power lost in the input distribution traces, I_{IN} is the input current to the converter, and R_{S_DIST} is the impedance of the input current distribution path (including copper traces and connectors). Decreasing the input voltage to keep D constant would increase Iin linearly. This would increase P_{LOSS} as a function of the square of I_{IN}, negatively impacting overall system efficiency.

A second evolving requirement for microprocessor power is small size. As CMOS fabrication capabilities continue to evolve it becomes possible to include more transistors on a die, and hence more functionality within a microprocessor chip. By the same token, the increased functionality applies to the motherboard as well, as increasingly complex microprocessors require increased memory, and peripheral devices (bus controllers, graphics processors, co-processors). The increasing device density leaves little room for the requisite power conversion and necessitates that the power conversion must not only cope with higher current output, but be smaller [2].

The key to small size for power conversion has long been in high switching frequency. A high switching frequency enables smaller magnetics, the largest component in typical power conversion systems by volume. Unfortunately there has long been a point of diminishing returns driven by the following equation:

$$P_{SW\_loss1} = F_{sw} \cdot Q_{g} \cdot V_{g} \qquad \text{[Eq. 3]}$$

where F_{SW} is the switching frequency, Q_{G} is the gate charge of the switching MOSFETs and V_{G} is the Gate voltage of the switching waveform. As the switching frequency increases, the switching losses increase as well, requiring a MOSFET with lower gate charge, or lower gate threshold. Such devices typically come with the penalty of a higher R_{dson}, thus increasing dissipative losses.

A second loss component that is directly proportional to switching frequency is described below [3]:

$$P_{SWloss2} = [\frac{1}{2}(T_{sw\_on} \cdot I_{sw} \cdot V_{sw}) +$$

$$\frac{1}{2}(T_{sw\_off} \cdot I_{sw} \cdot V_{sw})] \cdot f_{sw}$$

[Eq. 4]

In the equation above, T_{sw_on} and T_{sw_off} are the turn on and turn off times of the MOSFET, I_{sw} is the peak current through the MOSFET, V_{sw} is the voltage across the MOSFET when off and fsw is the switching frequency. Since the MOSFET does not instantaneously turn on or off, there are brief periods where the device will be dissipating power while transitioning off or on. The amount of power dissipated during these periods increases linearly with frequency.

2.0 Input Voltage Independent Solution with High Switching Frequency

The problems outlined above call for a solution with the following attributes:

1) High switching frequency to enable small size.

2) Decoupling of duty cycle from input and output voltage (as described in Eq. 1).

One added requirement that is imposed for the sake of pragmatism requires that any proposed system contain no additional penalties in terms of further power losses (contributing to overall inefficiency) or compromises that would affect the performance of the microprocessor load.

The proposed solution consists of a Sine Amplitude Converter ™ (SAC, Figure 1) at the point of load (microprocessor) powered by a ZVS Buck-Boost ™ regulator (Figure 7) from the 48V input. Both solutions with the external feedback and control loop are shown in Figure 9.

3.0 Sine Amplitude Converter – Point of load Conversion

The SAC uses a high frequency resonant tank to move energy from input to output [4]. The

resonant tank is formed by C_{res} (shown in Figure 1) and leakage inductance in the power transformer windings (designated P in the schematic). The four MOSFETs in the H-bridge are alternately switched at the resonant frequency of the tank. The presence of load current (+OUT to –OUT) creates resonant
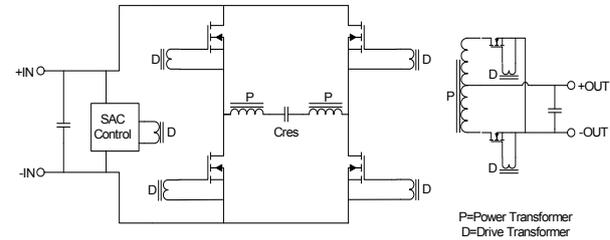
Figure 1: *Sine Amplitude Converter*

current through the tank, which is rectified by the two secondary switches and filtered by the output capacitance.

The SAC can be functionally distilled into the behavioral model shown in Figure 2. In this representation, several relationships become apparent.
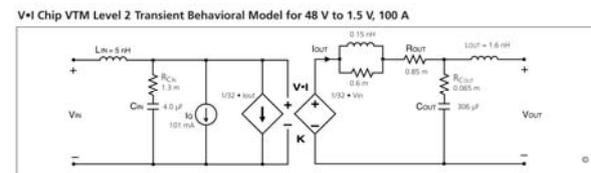
Figure 2: *Behavioral Model of SAC* [5]

At no load:

$$V_{OUT} = V_{IN} \cdot K$$
[Eq. 5]

K represents the "turns ratio" of the SAC. Rearranging Equation 5:

$$K = \frac{V_{out}}{V_{IN}}$$
[Eq. 6]

In the presence of load, V_{OUT} is represented by:

$$V_{OUT} = V_{IN} \cdot K - I_{OUT} \cdot R_{OUT}$$
[Eq. 7]

and I_{OUT} is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K}$$
[Eq. 8]

R_{OUT} represents the impedance of the SAC, and is a function of the R_{dson} of the input MOSFETs and the winding resistance of the Power transformer. By a similar token, I_Q represents the quiescent current of the SAC control and gate drive circuitry shown in Figure 1.

In a transformer based topology, V_{OUT} is a function of V_{IN}, not D. K is a constant and in order to provide a lower V_{OUT}, the Vin must be lowered. It should also be noted that K as a value can be very small. Unlike the Duty Cycle limitation where the functional limitation is in the ability to switch a MOSFET, K enables input to output ratios as large as 32:1 or greater.

The use of DC voltage transformation provides some additional interesting attributes. Assuming for the moment that R_{OUT} and IQ =0, equation 7 now becomes equation 6 and is essentially load independent. A resistor R_{IN} is now placed in series with V_{IN} as shown in Figure 3.
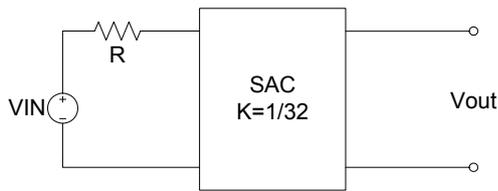
Figure 3: *Sine Amplitude Converter with series input resistor*

The relationship between V_{IN} and V_{OUT} becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \cdot R) \cdot K \qquad \text{[Eq. 9]}$$

Substituting the simplified version of Equation 8 (I_Q is assumed = 0) into Eq. 9 yields:

$$V_{OUT} = V_{IN} \cdot K - I_{OUT} \cdot R \cdot K^2 \qquad \text{[Eq. 10]}$$

This is similar in form to Eq. 7, where R_{OUT} is used to represent the characteristic impedance of the SAC. However, in this case a real R on the input side of the SAC is effectively scaled by K^2 with respect to the output.

There are several implications in the context of powering a microprocessor. Consider the SAC depicted in Figure 3. Assuming that R = 1Ω, the effective R as seen from the secondary side is .98mΩ. A 1 Ω upstream series input impedance essentially looks like 1mΩ.

A similar exercise should be performed with the addition of a capacitor, or shunt impedance, at the input to the SAC. A switch in series with V_{IN} is added to the circuit. This is depicted in Figure 4.
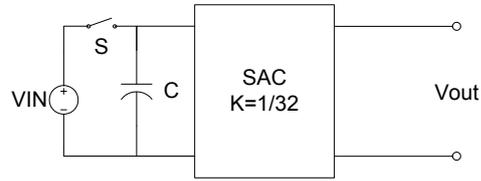
Figure 4: *Sine Amplitude Converter with input capacitor*

A change in V_{IN} with the switch closed would result in a change in capacitor current according to the following well known equation:

$$I_c(t) = C \frac{dV_{IN}}{dt} \qquad \text{[Eq. 11]}$$

Assume that with the capacitor charged to V_{IN}, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_c = I_{OUT} \cdot K \qquad \text{[Eq. 12]}$$

Substituting Equations 5 and 12 into Eq. 11 reveals:

$$I_{OUT} = \frac{C}{K^2} \cdot \frac{dV_{OUT}}{dt} \qquad \text{[Eq. 13]}$$

Once again, writing the equation in terms of the output has yielded a K^2 scaling factor for C, this time in the denominator of the equation.

Again, the implications for a low voltage, high current microprocessor application are worth considering. For a K factor less than unity, as shown in Figure 4, this results in an effectively larger capacitance on the output when expressed in terms of the input. With a K=1/32 as shown in Figure 4, C=1uF would effectively appear as C=1024uF when viewed from the output.

Low impedance is a key requirement for powering a high current, low voltage load efficiently. A switching regulation stage should have minimal impedance, while simultaneously providing appropriate filtering for any switched

currents. The use of a SAC between the regulation stage and the point of load provides a dual benefit, scaling down series impedances leading back to the source and scaling up shunt capacitance (or energy storage) as a function of its K factor squared. However, these benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables magnetic components to be small since magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies reduces core losses as well.

Switching losses defined in Eq. 4 appear as an increased series impedance if not minimized. In the SAC, switching losses are minimized by virtue of the fact that the voltage across C_{RES} in Figure 4 is a sinusoid. Therefore switching primary and secondary MOSFETs at the zero voltage transitions of the sinusoid, V_{SW} and hence $P_{SWLOSS2}$ in Eq. 4 is minimized. A practical implementation of a SAC can switch at up to 2MHz with overall efficiency >90% when converting 48-1.5Vdc at 100A [6].

Gate drive losses from Eq. 3 affect the quiescent current of the SAC (Iq in Figure 2). Here again, the 50% duty cycle of all MOSFETs can be used to an advantage. The gate drive energy from one phase of MOSFETs (primary and secondary rectifiers) can be used to drive the complementary pair. This reduces the quiescent losses to typically less than 2% of full load power output.

The impedance of the resonant bridge itself is effectively zero, hence R_{OUT} as a function of frequency of the SAC consists of a DC term, R_{OUT}, representing resistive terms (Rdson of switches, R of path lengths) and an AC term which is dominated by the package parasitic. A SAC with a K=1/32 can be implemented with a DC Rout of 1.0 milliohms and an AC impedance equivalent to 200pH. This has an impedance versus frequency as shown in Figure 5.
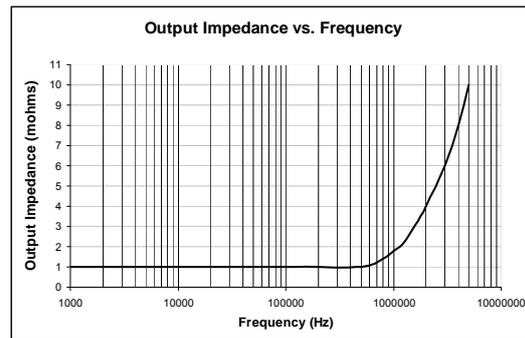
Figure 5: *Output impedance of K=1/32 SAC vs. Frequency.*

The Output impedance remains at the DC value until approximately 700KHz and by 1MHz it has only doubled. From the perspective of powering a microprocessor, ceramic capacitors would be used to keep the impedance at the microprocessor socket low beyond 1MHz, while the SAC would be used for everything below 1MHz. This eliminates the need for bulk capacitors at the point of load, since the Aluminum Polymer capacitors typically have 5 times the impedance of the SAC. The open loop response of a K=1/32 SAC to a 400A/us 100A load step is shown in Figure 6. In this case, there is no terminating capacitance on the output of the SAC, so the switching ripple can be clearly seen. Also visible is the response of the input to the load step, with a recovery of ~8us.
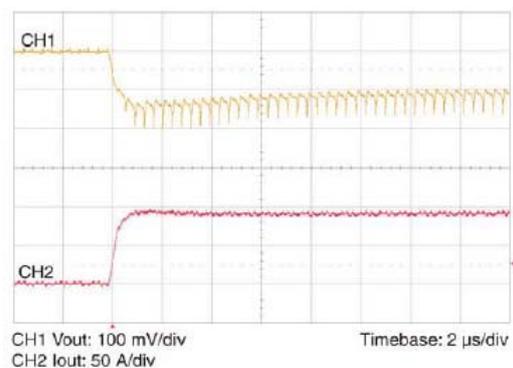
Figure 6: *Response of K=1/32 SAC to 100A load step.* [7]

It is important to note in the context of a microprocessor solution, that the open loop response of a SAC with K=1/32 closely resembles the required closed loop performance of an VRM powering a microprocessor with a load line (typically on the order of 1mΩ).

To conclude, a SAC as a point of load device enables high frequency, input voltage independent conversion with low impedance from DC – 1MHz.

4.0 Zero Voltage Switched Buck-Boost Stage

To power a microprocessor, a low impedance source is used to power the SAC.

As with the SAC, the key to low impedance lies in high frequency switching and minimizing the size of high frequency magnetics. It is also necessary to minimize initial conditions (such as continuous inductor current) at the start of each switching cycle.

The proposed topology for the regulation stage is a Zero Voltage Switched Buck Boost Regulator [8], shown in Figure 7.
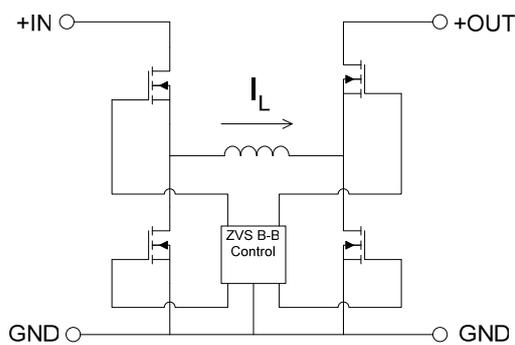
Figure 7: *Zero-Voltage Switched Buck Boost Converter*

The complete system is shown in Figure 9. A detailed work on the method of design of a high bandwidth control loop for this topology is forthcoming in a future paper. The attributes of this topology that support the goal of powering a low voltage high current microprocessor from 48V will be described here.

The ZVS Buck – Boost (ZVS B-B) converter is a discontinuous topology in which the inductor current, I_L, essentially returns to zero regardless of load. However, it is unlike a discontinuous topology in that the inductor current at the end of a cycle is slightly negative, thereby enabling zero voltage transitions on each of the four switches. As with the SAC, ZVS enables high frequency operation with high efficiency [9]. This also enables the ZVS B-B to maintain stability with a closed loop bandwidth theoretically in excess of 300Khz.

The ZVS Buck – Boost topology presents a single pole rolloff which enables simple Type 2 compensation. Type 3 compensation may be used in a system where high bandwidth is required and downstream parasitic impedances present phase shift at the crossover frequency.

A switching cycle for the ZVS B-B consists of four phases. In between phases, there is a ZVS delay between one MOSFET turning off and the next turning on. Each switching cycle consists of four phases, regardless of whether the ZVS B-B is boosting or bucking, as seen in Figure 8. Thus there is no delay or fundamental change in the control architecture when transitioning from one mode to another.
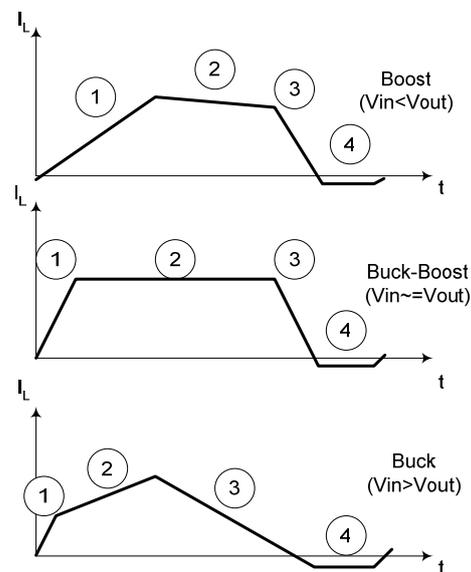
Figure 8: *Inductor current during 4 phases of a ZVS B-B switching cycle.*

5.0 Conclusion

The Sine Amplitude converter and ZVS Buck – Boost enable high frequency, efficiency and bandwidth while providing low voltage high current loads with high power density. The SAC presents a low impedance to the load, enabling
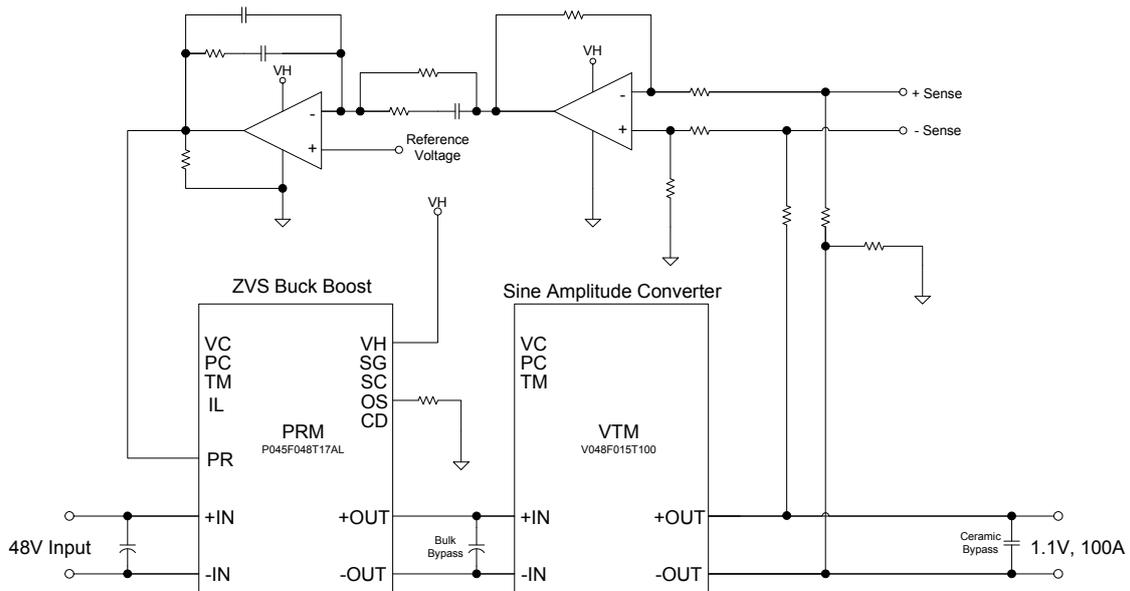
Figure 9 : *48-1.1V, 100A Solution using SAC and ZVS B-B*

reduction in POL capacitance, as well as high overall bandwidth.

Future work will detail a ZVS Buck – Boost compensation strategy that allows a control loop recovery of less than 5us to a load transient.

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