Application Note
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Prepared by:	Arendt Wintrich, Peter Beckedahl
Approved by:	Ulrich Nicolai

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Introduction of new IGBT Generation 7

1. Introduction

1.1 General Introduction

With this document SEMIKRON like to introduce the 1200V Generation 7 IGBT chips and their rollout to different power module packages. The new chip generation will be implemented from two independent sources. One source is Infineon which can be identified by the index "T7". The second source is a new chip supplier for SEMIKRON, which can be identified by the index "M7". Both IGBT types will be combined with the well-established SEMIKRON CAL4F freewheeling diode.

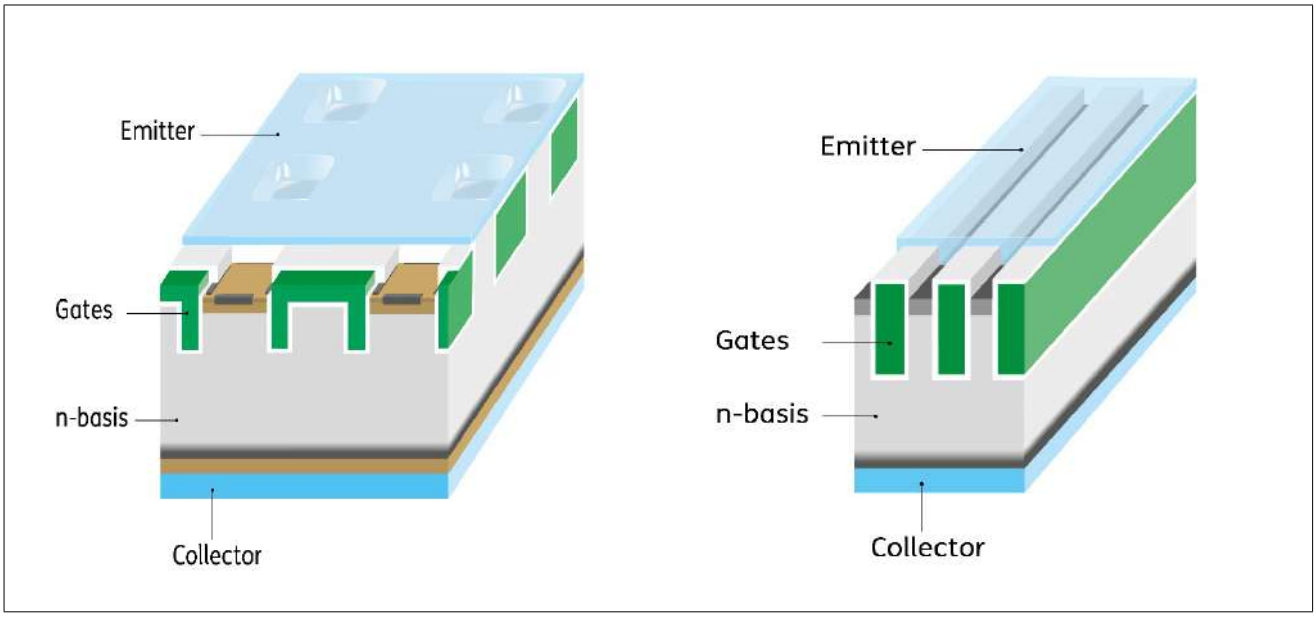
With the multiple chip source strategy, it is possible to select the best chip performance for the individual packaging platforms. Since the T7 IGBT has been optimized for low to medium power motor drive applications it will be first introduced in the low to medium power packages MiniSKiiP® and SEMITOP®. The

M7 IGBT is well suited for paralleling hence it will be introduced to the larger power module families SEMiX® and SEMITRANS®.

1.2 Chip Technology

The new chip generation is based on a significant increased cell density in conjunction with striped trench gate structures. The paralleled trench cell layout consists of active and passive trenches, which enable smaller cell pitches and very narrow mesa structures. This cell concept allows for higher carrier storage close to the emitter electrode, which leads to a significant increase in electrical conductivity in the drift zone. The main benefit is a substantial reduction of the forward voltage drop of up to 400mV compared to former chip generations based on squared trench cells, while the switching losses remain at a similar level like before.

Figure 1: Previous squared trench cell design and new striped trench gate structure



1.3 Main Advantages of IGBT Generation 7 based Power Modules

Due to reduced power losses, the new chip generation allows for a significant power density increase of up to 33%. A further power density increase can be obtained for overload conditions by raising the maximum chip operation temperature to 175°C. Next to the power density another important benefit is the improved environmental robustness of the new chip generation. The new chips pass the harsh HV-H3TRB (High Voltage, High Temperature, High Humidity Reverse Bias) test that assures reliable operation in hot and humid environment.

Main advantages are:

- 20% lower on-state voltage
- Operation junction temperature of 175° during overload
- High humidity robustness
- 33% higher power density in same package
- 8µs short circuit robustness
- Safe operation with 0 volts gate turn-off

1.4 Parameter Overview

Figure 2 gives an overview of the relevant chip parameters for different chip types. The on-state voltage reduction allows for a 25% chip shrinkage at same current rating. As a trade-off for the superior power density, the short circuit withstand time t_{SC} had to be reduced to 8µs. This is already known from other recent chip generations and still provides sufficient safety margins for modern protection topologies.

IGBT chips can be optimized for multiple application purposes based on a given technology curve. A trade-off can be made between low switching losses for high frequency applications and low conduction losses if high power is the main target. Another important selection criterion for high current modules is an equal current sharing and no oscillations between paralleled chips. The new Generation 7 IGBTs have been matched to replace the existing IGBT4 based products.
The T7 IGBT has been optimized for motor drive applications from low to medium power. The IGBT maintains low switching losses even with low voltage transients of 5kV/µs, which is a typical limit for electric motors. It will be implemented in SEMITOP® and MiniSKiiP® CIB and AC (sixpack) modules, covering a current range from 10A up to 200A.
The M7 IGBT is a medium to high power chip which can be paralleled easily making it the ideal candidate for high power module families SEMiX® and SEMITRANS® with sixpack, half-bridge and 3-Level configurations covering power ratings up to MW range.

Table 1: Parameter Overview of IGBT4 and IGBT Generation 7 Chip Versions

100A Chip Rating	F4	T4	E4	T7	M7
$V_{CE(sat)}$ 25°C	2.05V	1.75V	1.75V	1.6V	1.6V
$V_{CE(sat)}$ @150°C	2.6V	2.2V	2.05V	1.8V	1.85V
E_{sw}/100A @150°C	15mJ	21mJ	24mJ	21mJ	22mJ
E_{on}/100A @150°C	7mJ	11mJ	11mJ	10mJ	11mJ
E_{off}/100A @150°C	8mJ	10mJ	13mJ	11mJ	11mJ
Q_G (V_{GE} -8V/+15V)	0.6µC	0.6µC	0.6µC	1.7µC	1µC
Chip Area	100mm²	100mm²	100mm²	75mm²	75mm²
t_{SC} @150°C, 800V	10µs	10µs	10µs	8µs	8µs

2. Application of Generation 7 IGBT

2.1 Switching behaviour

In general the switching behaviour is similar to the previous generation IGBT4. The gate controls the turn-on behaviour, but the turn-off behaviour is controlled in wide ranges by the external circuit only.

2.1.1 Turn-on

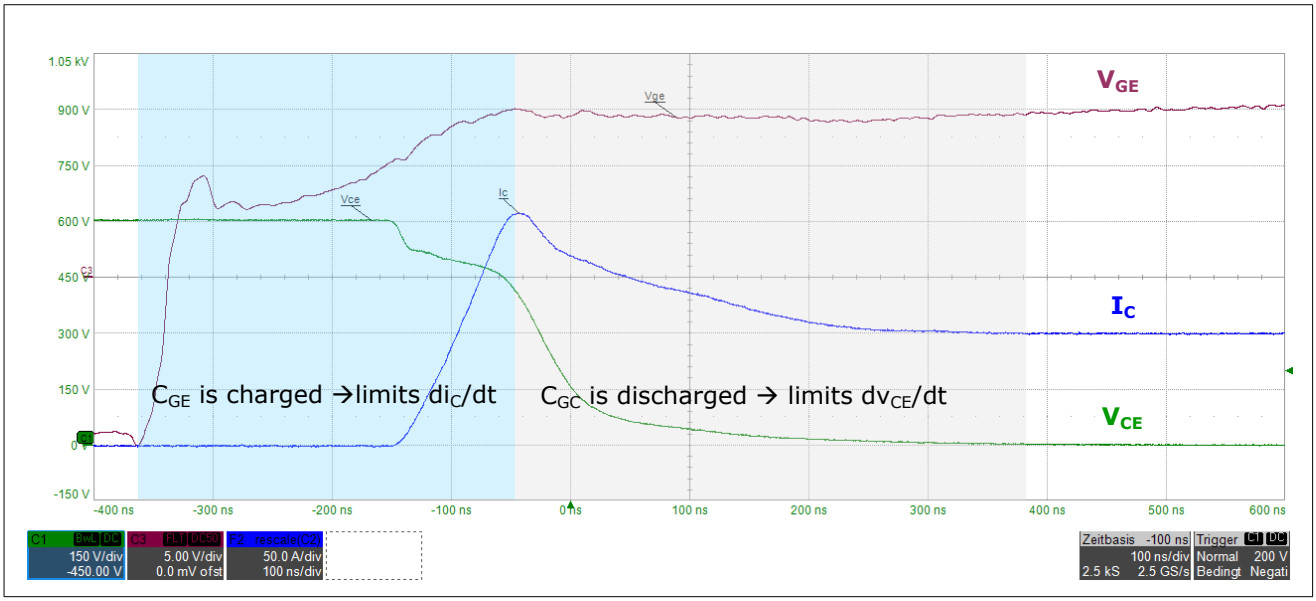
In most cases the supply voltage V_{GG} of the driver and the gate resistor R_G determine the charging process of the gate:

$$i_G(t) = \frac{V_{GG} - v_{GE}(t)}{R_G}$$

The faster the gate is charged, the higher the di_C/dt of the collector current and the higher the dv_{CE}/dt of the collector-emitter-voltage becomes. New for the IGBT Generation 7 is the high ratio between a small Miller-capacitance C_{GC} at high V_{CE} and a large gate emitter capacitance C_{GE}. When the gate voltage exceeds the threshold voltage only C_{GE} is charged by i_G. A high i_G (low R_G) is necessary to achieve a reasonable di_C/dt and low turn-on losses E_{on}. The small Miller-capacitance C_{GC} is discharged during the following plateau phase of V_{GE} and the same low R_G leads to high dv_{CE}/dt in that case.

In general fast switching is possible and very low turn-on switching losses can be achieved if high dv_{CE}/dt is acceptable for the application. If necessary, a compromise has to be found between dv_{CE}/dt and E_{on}.

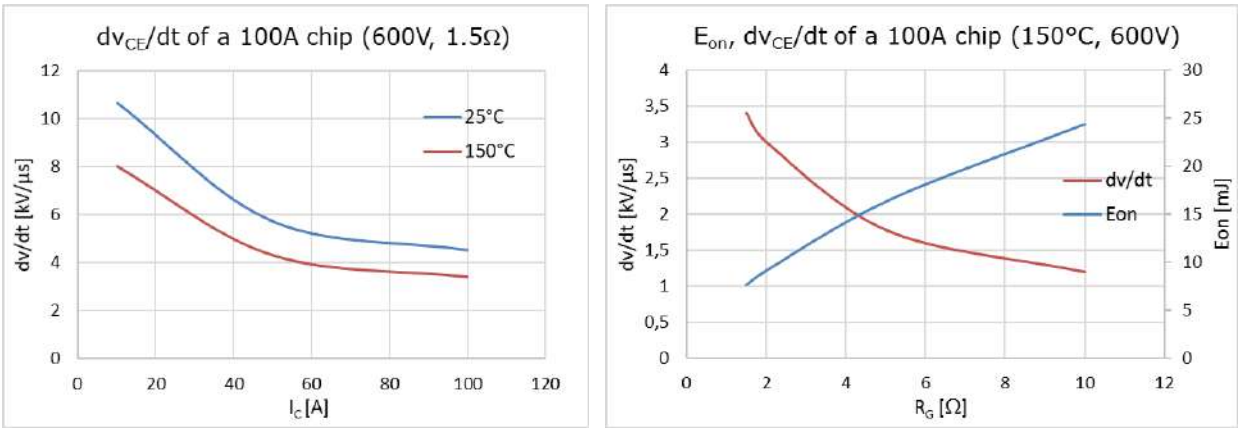
Figure 2: Turn-on at $I_{C(nom)}$=100A, V_{CC}=600V, T_j=150°C and R_G=1.6Ω



When comparing statements about dv_{CE}/dt it is important to know the definition for the measurement conditions. A measurement between 90% and 10% of V_{CC} results in lower values, possibly only 2/3 of a 80%...20% measurement. Measurements in a window around 30% of V_{CC} would result in the highest dv_{CE}/dt values. Figure 3 shows typical dv_{CE}/dt values for the commonly used 10%-90% V_{CC} definition of a 100A IGBT T7. At low temperatures and low currents the dv_{CE}/dt has the highest value.

IGBT M7 shows a similar behaviour, but for different external gate resistor values because the internal $R_{G(int)}$ and the gate charge Q_G are different.

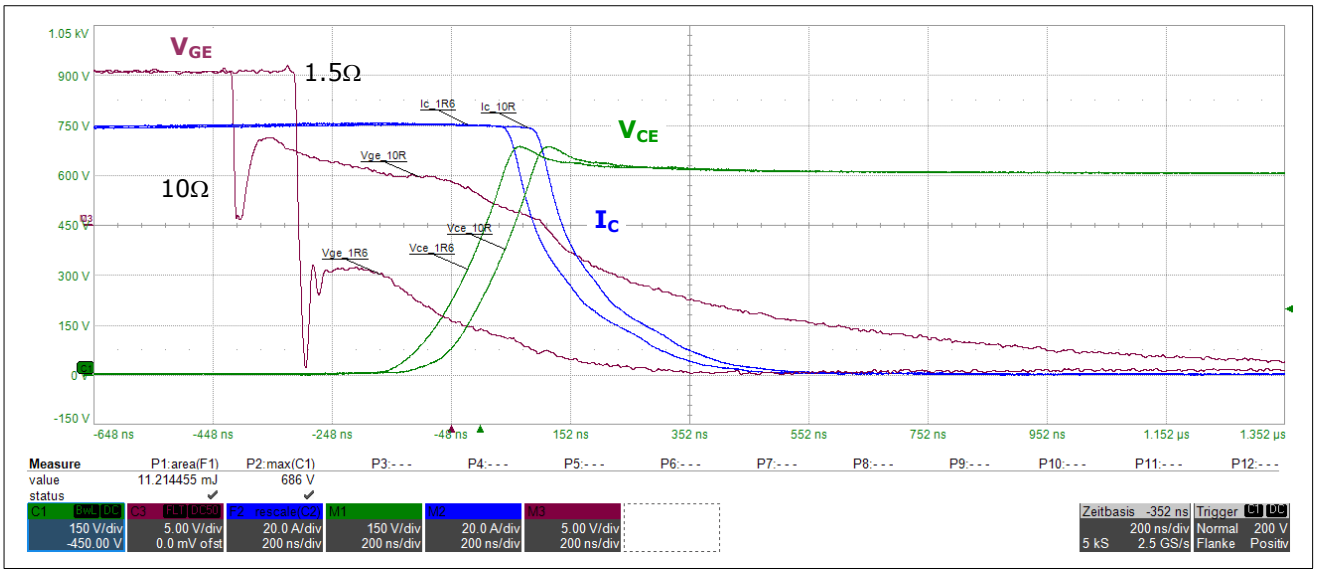
Figure 3: dv_{CE}/dt behaviour at turn-on for different conditions



2.1.2 Turn-off

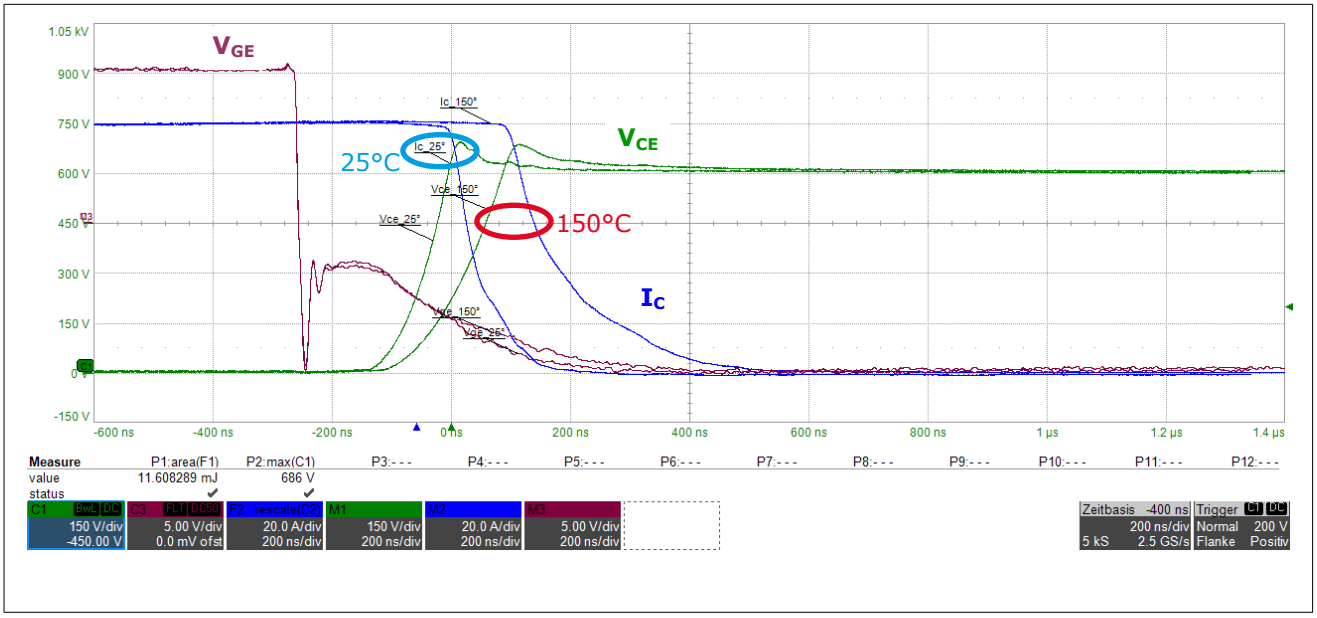
Under nominal switching conditions the gate channel is already closed ($v_{GE}(t) < V_{GE(th)}$) before V_{CE} starts to rise and before I_C starts to fall (see Figure 4). The high amount of charge carriers in the base of the semiconductor is comparable to a big capacitor $C_{n\text{-base}}$, which feeds the collector current. The turn-off behaviour is independent from R_G in a certain range typically given in data sheet characteristics. Only a different turn-off delay time in the gate voltage (violet) is visible when changing R_G. Nevertheless the time response of I_C (blue) and V_{CE} (green) are identical for R_G=1.6Ω and R_G=10Ω. Consequently also the turn-off losses are almost independent of R_G. The two curves are shifted slightly to see that both voltage and current signals are running in parallel. At turn-off the I_C determines the dv_{CE}/dt: the higher the I_C is, the faster $C_{n\text{-base}}$ is discharged; low currents lead to low dv_{CE}/dt.

Figure 4: Turn-off at $I_{C(nom)}$=100A, V_{CC}=600V, T_j=150°C and R_G=1.6Ω compared to 10Ω



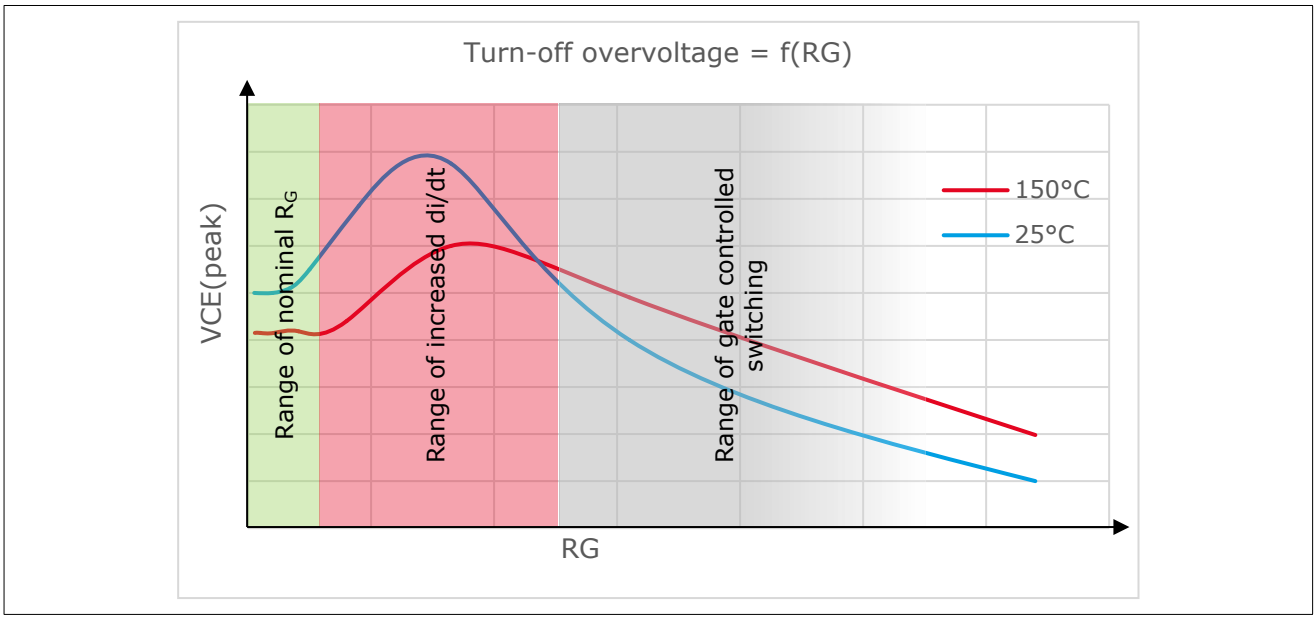
At turn-off the dv_{CE}/dt is highest at low temperatures and maximum current. In the example in Figure 5, the dv_{CE}/dt increases by 50% from 3.4kV/µs at T_j=150°C to 5.1kV/µs at 25°C.

Figure 5: Turn-off at $I_{C(nom)}$=100A, V_{CC}=600V, R_G=1.6Ω, T_j=25°C and T_j=150°C



The delay time increases for even higher R_G and free charge carriers disappear during that time. This leads to less tail current and an increased di_C/dt with a higher turn-off overvoltage (red range in Figure 6). A gate controlled turn-off behaviour is achievable only for very high R_G values but to the disadvantage of high switching losses and a very long delay time in active mode. Therefore relative low R_G values are recommended to assure low switching losses and a low overvoltage.

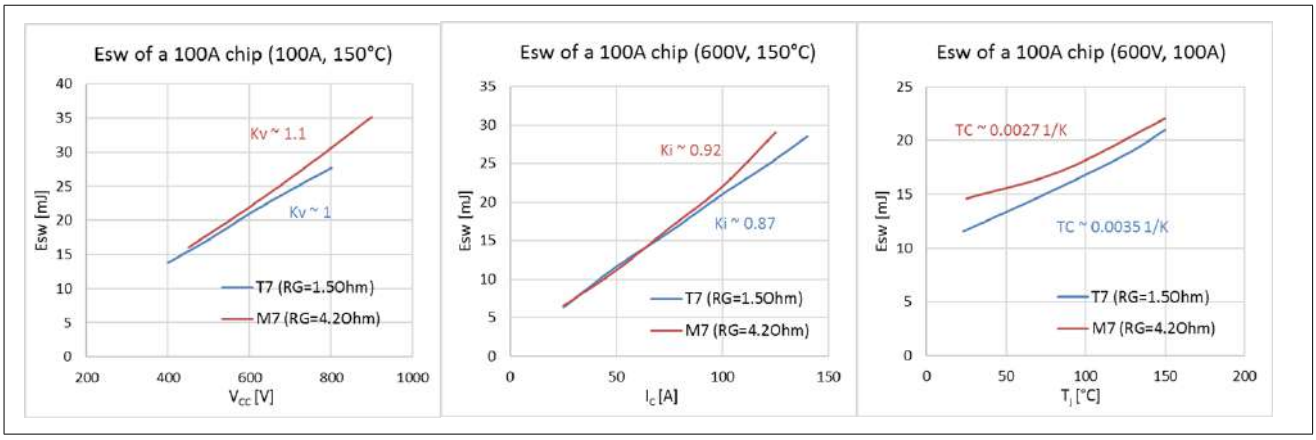
Figure 6: Principle behaviour of turn-off overvoltage for different R_G at T_j=25°C and T_j=150°C



2.1.3 Switching loss dependency on temperature, voltage and current

Interdependencies of various parameters are necessary for loss calculation and simulation (see [2], page 277ff). While the dependencies on current and gate resistor are stated in the data sheet, dependencies on voltage and temperature are missing. The voltage dependency is almost linear for both IGBTs (voltage exponent around 1) and thereby much lower compared to former generations. The switching losses at room temperature are roughly 40% lower compared to 150°C (TC~0.003·1/K)

Figure 7: Dependencies of switching losses from operation conditions $E_{sw}=E_{on}+E_{off}$



2.1.4 Short circuit

Both Generation 7 IGBTs are able to turn-off a short circuit current. Due to the chip shrinkage and therewith a lower thermal chip capacity the short circuit pulse duration t_{SC} is shorter than with former IGBT generations. It is specified for V_{CC}=800V and V_{GE}=15V with t_{SC}=8µs at 150°C and t_{SC}=7µs at 175°C.

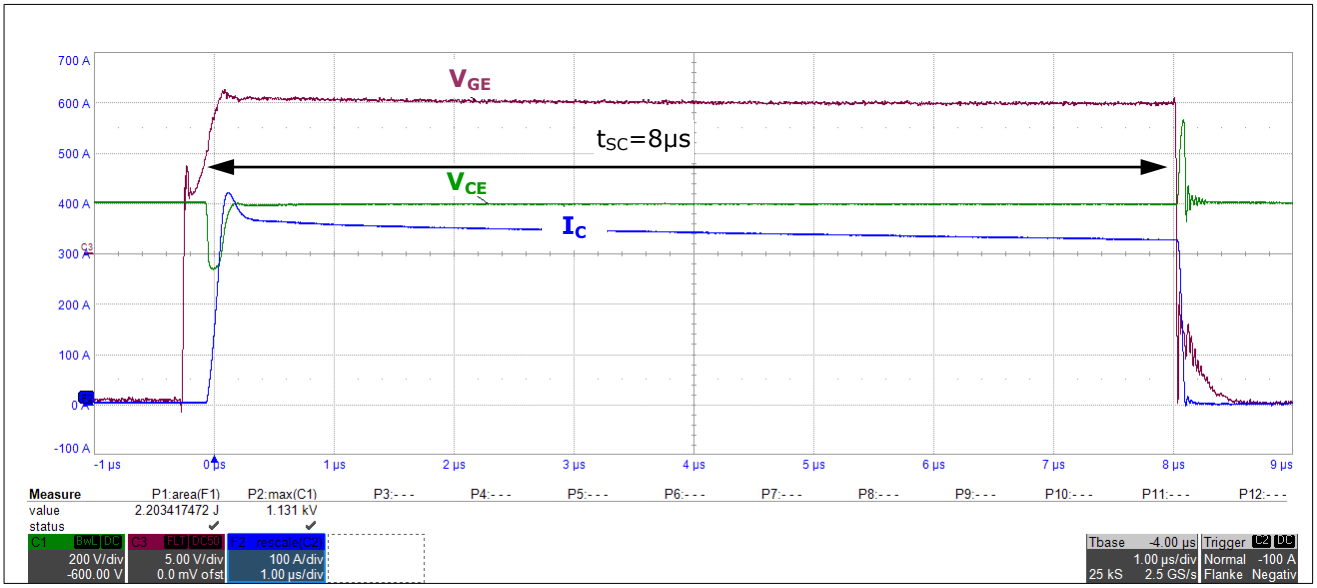
This statement specifies a certain energy $E_{SC} = I_{SC} \cdot V_{CC} \cdot t_{SC}$. The short circuit current is self-limiting at V_{GE}=15V and T_j=150°C to about $4 \cdot I_{C(nom)}$ (i.e. E_{SC}=2.56J for a 100A chip). Short circuit parameters can be varied to some extend while keeping the energy constant, like shown in the two following examples. The influencing factors can be superimposed. In example 1 the DC-link voltage is only 600V instead of 800V and by this the t_{sc} can be increased to:

$$t_{SC}(600V) = t_{SC}(800V) \cdot \frac{800V}{600V} = 10.6\mu s.$$

In example 2 a higher short circuit current is considered, because the IGBT might be controlled by a higher gate voltage. The current is increased by 25% ($5 \cdot I_{C(nom)}$) at V_{GG}=17V and t_{sc} has to be reduced consequently to:

$$t_{SC}(17V) = t_{SC}(15V) \cdot \frac{4 \cdot I_{C(nom)}}{5 \cdot I_{C(nom)}} = 6.4\mu s.$$

Figure 8: Short circuit of $I_{C(nom)}$=100A chips at V_{CC}=800V, T_j=150°C



Short circuit turn-off with nominal R_G without any clamping or soft turn-off option is possible in many cases. A low inductance, state of the art DC-link is mandatory but it is necessary to verify the short circuit performance in the final application setup.

2.2 Gate Capacitance

The Generation 7 IGBT chips have a significant higher gate capacitance compared to previous IGBT generations due to the new striped trench gate structure. Depending on the gate turn-on and turn-off voltages this might lead to higher gate charges, compared to former chip generations (see Table 1).

The gate input capacitance C_{ies} is divided into the gate-emitter capacitance C_{GE} and the gate-collector (Miller) capacitance C_{GC}. Figure 9 shows the equivalent circuit diagram of an IGBT including the parasitic capacitors. The increased C_{ies} value can be solely attributed to an increased C_{GE} value while the Miller capacitance C_{GC} remains at a low level.

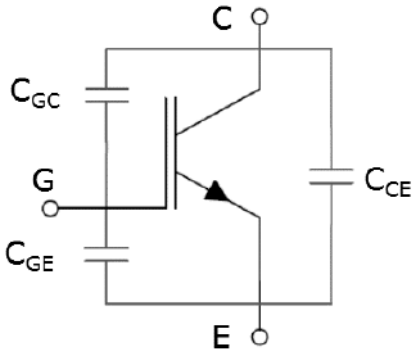
The combination of a large gate-emitter and a relatively small gate-collector capacitance makes the IGBT Generation 7 very robust against undesired parasitic turn-on. This effect is usually induced from diode switching transients, which charge the gate through the Miller capacitance [3].

Additional external gate-emitter capacitors or a negative turn-off gate voltage to keep the gate at a safe state are not necessary for many applications. Small to medium size power modules can be well controlled with a unipolar gate supply voltage of +15V / 0V [4]. A unipolar supply voltage keeps the driver design simple and reduces the required driver power to similar levels needed for former chip generations [3].

The required gate drive power is calculated with the equation below. Q_G depends on the chosen gate drive voltages and can be derived from the graphs in the datasheet.

$$P_{GD(out)} = Q_G \cdot (V_{G(on)} - V_{G(off)}) \cdot f_{sw}$$

Figure 9: Equivalent circuit diagram of IGBT and capacitive elements



	IGBT
Input capacitance	$C_{ies} = C_{GE} + C_{GC}$
Reverse transfer capacitance (Miller capacitance)	$C_{res} = C_{GC}$
Output capacitance	$C_{oes} = C_{GC} + C_{CE}$

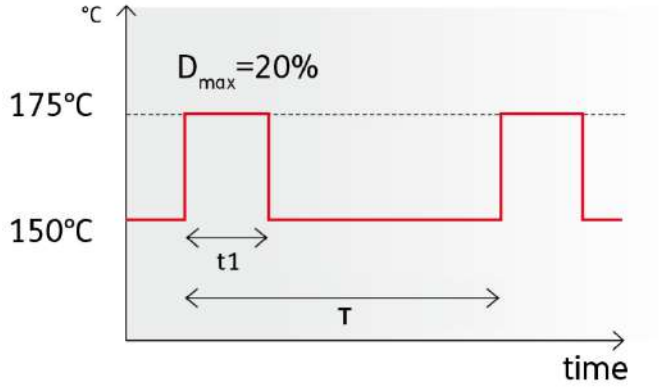
2.3 Operation junction temperature up to 175°C

The new Generation 7 IGBTs allow a maximum operation at $T_{j(op)-ol}$=175°C during overload. Figure 10 shows details of the maximum temperature definition and the allowed load profile. The nominal continuous operation is limited to a maximum junction temperature of $T_{j(op)}$=150°C.

However to match typical motor drive overload profiles it is allowed to exceed $T_{j(op)}$=150°C to up to $T_{j(op)-ol}$=175°C for an absolute maximum time of t_1=60s. In addition the overload duration is limited to a maximum duty cycle of 20%.

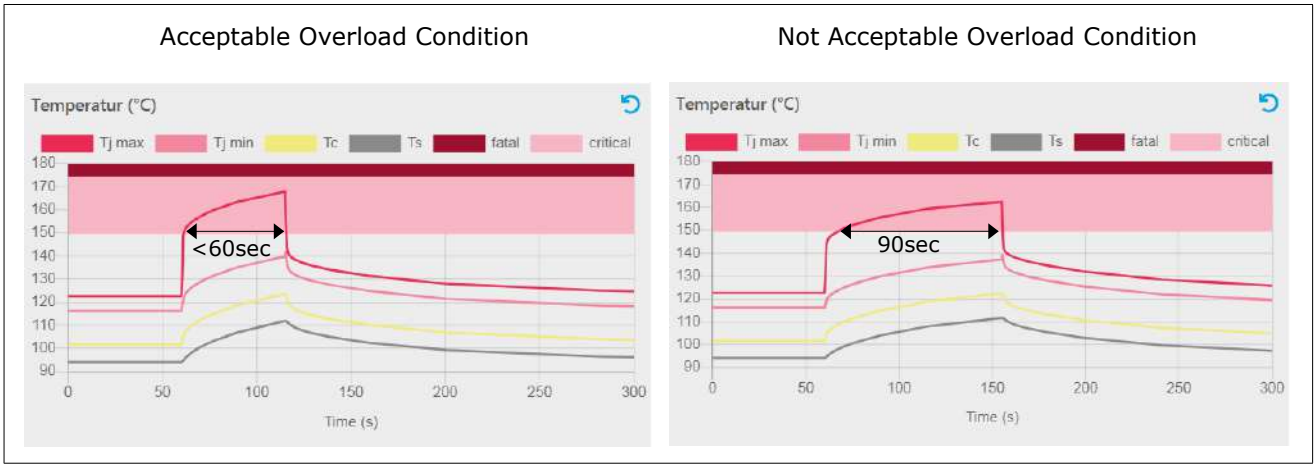
Example: The overload time t_1 is limited to an absolute maximum duration of 60s, so the minimum permissible cycle time T is 300s or larger. If the load cycle time T is 25s the permissible overload with 150°C<$T_{j(op)-ol}$<=175°C is limited to t_1<=5s.

Figure 10: Definition of maximum operational junction temperature



It is important to notice that the maximum junction temperature should never exceed 175°C including the temperature ripple originating from the fundamental output frequency. The lower the fundamental output frequency of an inverter the higher the temperature ripple in the junction becomes. The effect can be seen in Figure 11 for a standard 2-level inverter on an air-cooled heatsink. At nominal load the fundamental output frequency is set to 50Hz which results in a moderate junction temperature swing of 7K. During overload condition, the current is increased and at the same time also the fundamental output frequency is reduced to 10Hz. This leads to a temperature swing of more than 25K.
The example on the left fulfils the defined overload conditions: The junction temperature never exceeds 175°C, exceeds 150°C for less than 60s and the duty cycle is lower than 20%.
The example on the right does NOT fulfil the defined overload conditions: The junction temperature is even lower than in the previous example, but the junction temperature exceeds 150°C for about 90s. Additionally the duty cycle is 30%.

Figure 11: Example of acceptable and not acceptable overload condition



This overload definition is in particular beneficial for drives with well-defined load cycle conditions. Also fault situations e.g. low voltage ride-through can be covered without limiting the nominal operation.

2.3.1 Further considerations for operation at higher junction temperatures

Higher junction temperatures will lead to higher heatsink temperatures, which could imply additional limitations for the power module as well as other system components:

- Solder and wire bond connections in power modules are aging over time. The dominating factor is the junction temperature swing during load cycles. This is particular critical for servo and elevator drives as well as wind turbines. It is recommended to perform a lifetime calculation based on the mission profile of critical applications in order to verify the expected service life.
- An additional limitation is the maximum permissible power module case (or plastic housing) temperature, which can be found in the module datasheet. This can be in particular critical for long overload durations of air-cooled systems where the heatsink is subject to an additional temperature rise.
- The maximum heatsink temperature underneath the power module will also effect the Thermal Interface Material (TIM). Please check the maximum permitted operation condition in the relevant TIM datasheet. [5]
- Power modules with higher power density and higher maximum junction temperature allow for a higher inverter current in the same footprint. This could lead to additional losses and heating in bus bars or the power PCB. Losses in the PCB and maximum temperatures of the PCB components need careful considerations. High temperature PCB materials, wider copper tracks, thicker copper layers or additional number of layers as well as thermal vias should be taken into account.

2.4 HV-H3TRB Robustness

Another major benefit of the new IGBT chip Generation 7 is the increased robustness against high humidity environments. This is an important feature to improve the reliability for outdoor applications with changing load cycles and rough climatic conditions. All power modules based on IGBT Generation 7 chips have been subject to a HV-H3TRB test based on IEC 60068-2-67 and IEC 60749-5. The improvement is possible thanks to a revised chip edge termination structure.

Test conditions:

- Test voltage: $0.80 \cdot V_{CES}$ e.g. $960V_{DC}$ for 1200V chips
- Ambient temperature: $T_{amb}=85°C$
- Ambient relative humidity: RH=85%
- Gate voltage: $V_{GE}=0V$
- Duration: 1000 hours

Please note that the environmental specification of IGBT Generation 7 based power modules remain unchanged. Condensation is not allowed during operation. Please refer to [6] for detailed explanation about humidity and condensation effects in power electronic systems.

2.5 Practical recommendations

2.5.1 Chip shrinkage and current rating

Generation 7 IGBTs have significantly reduced conduction losses, which enabled a chip shrinkage of about 25%. In turn smaller chips lead to higher thermal resistance and potentially higher junction temperatures.

The new chips are sized carefully in such way that chip shrinkage and loss reduction compensate each other. This means that a Generation 7 IGBT with the same nominal chip current rating achieves also the same output power as the former generation although it provides lower losses.

On the other hand higher current ratings in the same power module package are possible. This allows for about 20% higher output power keeping the losses comparable to the former module generation. The heatsink does not need improvement since the losses are not increasing.

2.5.2 Cross-reference to IGBT4 based power modules

As described before it is easy to compare IGBT 4 based power modules with the new IGBT Generation 7 based power modules. Power modules with the same nominal current rating can also drive the same output power. A cross-reference table is not needed.

2.5.3 Gate resistor selection

The datasheet provides switching loss data for external gate resistors at typical gate voltages of V_{GE} = +15/-15V. Larger power modules have additional internal gate resistors R_{Gint}, which are integrated into the IGBT chips to assure good current sharing between paralleled chips.

Since IGBT Generation 7 based power modules have a larger gate capacitance also the chip internal gate resistors have been reduced to assure similar charging times while keeping a good gate stability. This reduction can be significant and will lead to higher gate peak currents. Inverter designers should confirm the maximum peak current capability of the gate driver. An additional booster circuit might be necessary to provide sufficient peak currents.

2.5.4 Repetitive peak collector current

The repetitive peak collector current I_{CRM} corresponds to the maximum pulsed collector current of the IGBT chip multiplied by the number of parallel chips per switch, limited by T_{jmax}. I_{CRM} is fixed to 2 times the nominal current rating $I_{C(nom)}$ for all new Generation 7 IGBT modules. This parameter is independent from the pulse duration and must not be exceeded even if the maximum chip temperature is not reached.

Under normal operation conditions even with sever overloads these limits will not be reached. Special attention should be paid to very small T7 IGBT based power modules operating with high capacitive cable loads [7]. At high junction temperatures the T7 IGBT starts already to move out of the linear saturation voltage characteristic close to the I_{CRM} limit. It is possible that high turn-on peak currents from capacitive cable loads come close to the I_{CRM} limit. This might lead to additional turn-on and conduction losses of small T7 modules. A step to a higher current rating module might be necessary.

3. Performance comparison

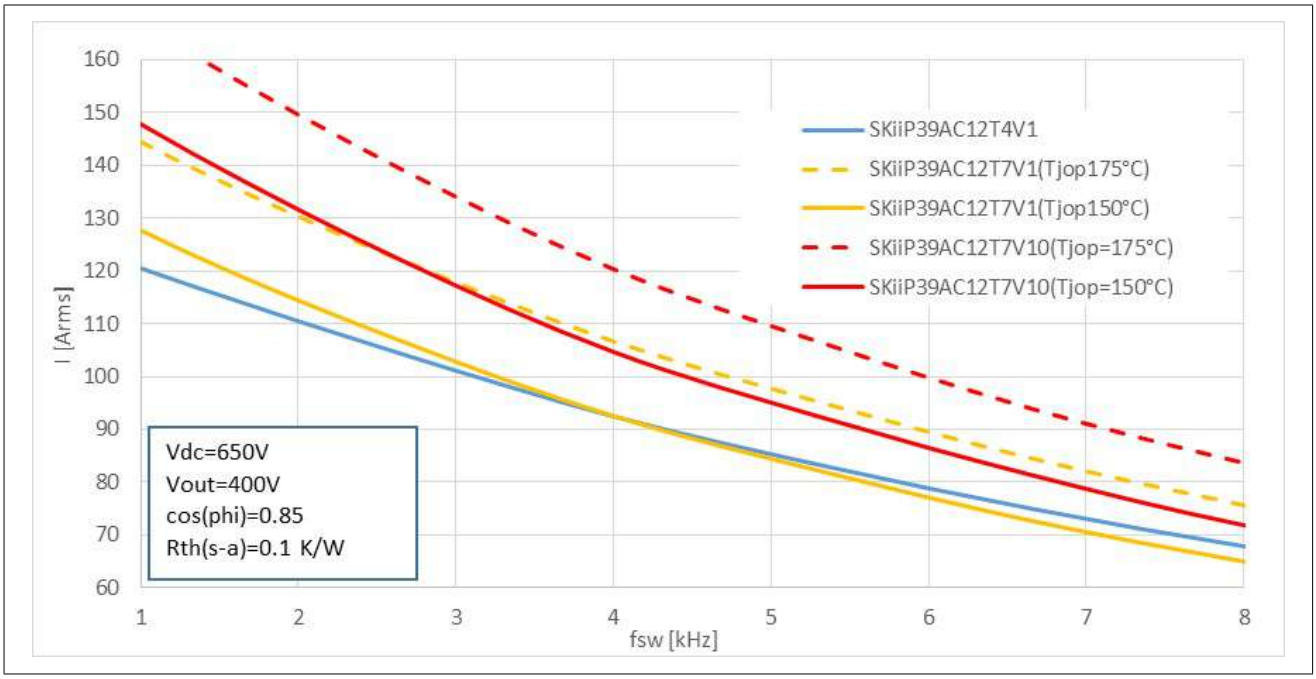
3.1 MiniSKiiP

Table 2 and Figure 12 shows a comparison of a 150A rated T4 based MiniSKiiP 3 with T7 versions for a theoretical maximum continuous inverter current at $T_{j(op)}$ =150°C. The 150A rated T7 device with the same nominal current achieves a similar inverter output current at switching frequencies f_{sw} of 4kHz with some advantages for lower f_{sw}. A 200A rated T7 device in the same housing allows 10 to 15% higher inverter currents for the same operation temperature of 150°C. The dashed curves show the additional theoretical overload current which is possible due to the increased maximum chip temperature of $T_{j(op)\ max}$ =175°C for the T7 versions during overload.
V_{dc}=650V; V_{out}=400V; f_{out}=50Hz; cos(phi)=0.85; No additional overload;
cooling with a typical air-cooled heatsink with $R_{th(s-a)}$=0.1K/W

Table 2: Comparison of maximum inverter currents for IGBT T4 and T7 at f_{sw}=4kHz

Module	$I_{C(nom)}$ [A]	I_{out} [Arms]	I_{out} Ratio to T4	$T_{j(op)\ max}$ [°C]
SKiiP39AC12T4V1	150	92	100%	150
SKiiP39AC12T7V1	150	92	100%	150
		106	115%	175
SKiiP39AC12T7V10	200	104	113%	150
		120	130%	175

Figure 12: Maximum inverter current MiniSKiiP 3 as a function of switching frequency



3.2 SEMiX3p

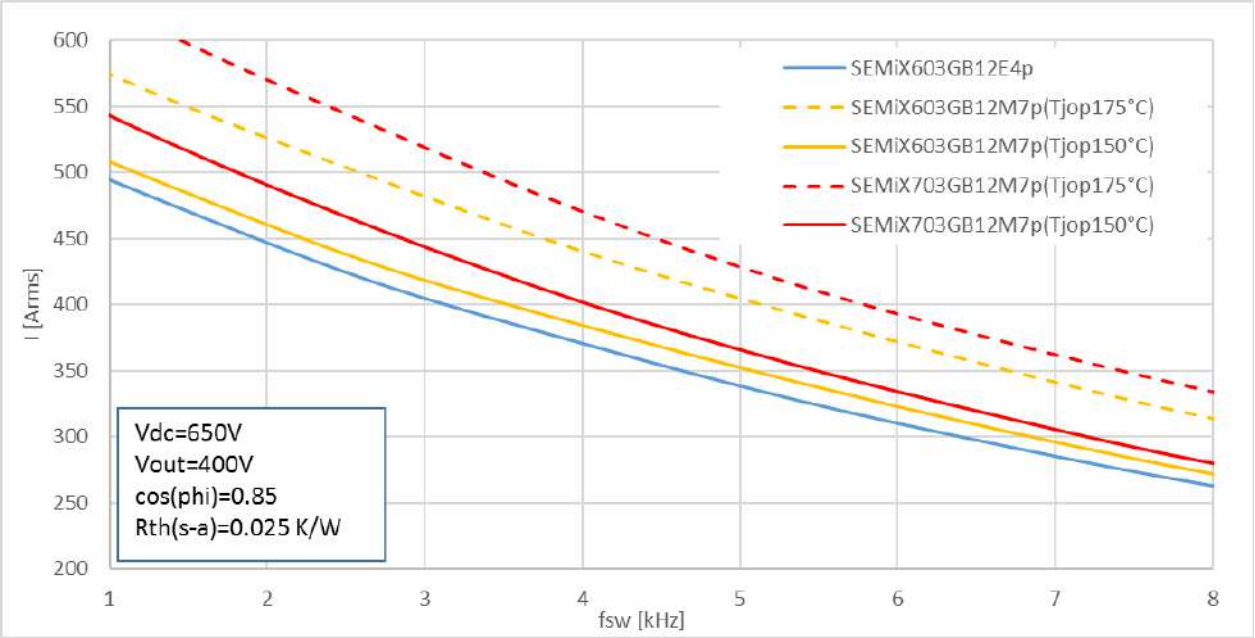
Table 3 and Figure 13 show a comparison of a 600A rated IGBT E4 based SEMiX 3 Press-Fit with M7 versions for a theoretical maximum continuous inverter current at $T_{j(op)}$ =150°C. The 600A rated M7 device with the same nominal current achieves slightly higher inverter output current over a wide switching frequency range. The 700A M7 device in the same housing allows 10% higher inverter currents for the same operation temperature of 150°C. The dashed curves show the additional theoretical overload current which is possible due to the increased maximum chip temperature of $T_{j(op)\ max}$ =175°C for the M7 versions during overload.

V_{dc}=650V; V_{out}=400V; f_{out}=50Hz; cos(phi)=0.85; No additional overload;
cooling with a typical air-cooled heatsink with $R_{th(s-a)}$=0.025K/W

Table 3: Comparison of maximum inverter currents for IGBT E4 and M7 at f_{sw}=4kHz

Module	$I_{C(nom)}$ [A]	I_{out} [Arms]	I_{out} Ratio to E4	$T_{j(op)\ max}$ [°C]
SEMiX603GB12E4p	600	370	100%	150
SEMiX603GB12M7p	600	384	104%	150
		440	119%	175
SEMiX703GB12M7p	700	402	109%	150
		470	127%	175

Figure 13: Maximum inverter current SEMiX 3 Press-Fit as a function of switching frequency



4. Summary

IGBT Generation 7 power modules offer many advantages over former generation modules. Most important are the reduced losses, which enable either higher inverter efficiency or higher power density. Higher overload operational junction temperatures can further increase the power density, in particular for applications with well-defined short-term overloads or fault ride-through conditions. Many applications will additionally benefit from the improved humidity robustness of the new chip generation. The switching behaviour and dv_{CE}/dt is well controlled by the gate. In many cases it is possible to turn-off short circuit conditions with standard gate resistors, a soft turn-off might not be necessary any more.

Some points need to be considered during the system design. The gate capacitance of the Generation 7 IGBT modules is significantly higher than in former module generations. This will lead to a higher gate driver power and occasionally to a higher gate peak current demand. In turn the increased C_{GE} can be beneficial for many, mainly low power applications: additional external gate-emitter capacitors and a negative turn-off voltage are not needed anymore. A unipolar gate driver makes the circuit design simple and it reduces the required gate driving power.

Figures and Tables

Symbols and Terms

Letter Symbol	Term
C_{GC}, C_{GE}, C_{ies}	IGBT gate to collector (Miller) capacitance, gate to emitter capacitance, input capacitance (output short circuited)
$C_{n\text{-}base}$	Virtual capacitor representing the stored charge in the n-base region
cos(phi)	Power factor
D, D_{max}	IGBT duty cycle, maximum allowed duty cycle for T_j=175°C
di_C/dt	Rate of rise of collector current
dv_{CE}/dt	Rate of fall of collector-emitter voltage
E_{sw}, E_{on}, E_{off}	IGBT total switching loss, turn-on switching loss, turn-off switching loss
f_{out}, f_{sw}	Inverter fundamental output frequency, IGBT switching frequency
HV-H3TRB	High voltage, high humidity, high temperature reverse bias test
I_C, $i_C(t)$	Collector current, time dependent collector current
$I_{C(nom)}$, I_{CRM}	Nominal IGBT chip current, repetitive peak collector current
I_{SC}	Collector current at short circuit
I_G, $i_G(t)$	Gate current, time dependent gate current
I_{out}	Inverter output RMS current
$P_{GD(out)}$	Gate driver power
Q_G	IGBT gate charge
R_G, R_{Gint}	Total gate circuit resistance, module-internal gate resistor
RH	Air humidity
$R_{th(s\text{-}a)}$	Thermal resistance heatsink to ambient
T, t_1	Duration of period, overload pulse duration
TC	Temperature coefficient
T_{amb}	Ambient Temperature
T_j, $T_{j(op)}$, $T_{j(op)\text{-}ol}$, $T_{j(op)\text{-}max}$	Junction temperature, operating junction temperature, overload operating junction temperature, maximum operating junction temperature
t_{SC}, E_{SC}	Short circuit withstand time, short circuit withstand energy
V_{GE}, $v_{GE}(t)$, $V_{GE(th)}$	Gate-emitter voltage, gate-emitter threshold voltage
$V_{G(on)}$, $V_{G(off)}$	Turn-on and Turn-off gate voltage level (driver)
V_{CC}, V_{GG}	Collector-emitter supply voltage, gate-emitter supply voltage
V_{dc}	Inverter DC input voltage

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors", page 436ff [2]

References

[1] www.SEMIKRON.com

[2] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, "Application Manual Power Semiconductors", 2nd edition, ISLE Verlag 2015, ISBN 978-3-938843-83-3

[3] U. Schilling, P. Beckedahl, "Comparative Study on the Dynamic Behavior of Next Generation IGBT Modules and Freewheeling Diode Optimization" PCIM Europe, Nuremberg, 2018

[4] SEMIKRON Application Note AN 1401 "Limits and hints how to turn off IGBTs with unipolar supply"

[5] SEMIKRON Technical Explanation "Thermal Interface Materials"

[6] SEMIKRON Application Note AN 16001 "Effect of Humidity and Condensation on Power Electronics Systems"

[7] SEMIKRON Application Note AN 17002 "Influence of capacitive cable load on switching losses"

IMPORTANT INFORMATION AND WARNINGS

SEMIKRON INTERNATIONAL GmbH
Sigmundstrasse 200, 90431 Nuremberg, Germany
Tel: +49 911 6559 6663, Fax: +49 911 6559 262
sales@semikron.com, www.semikron.com