WHITE PAPER

# High Performance ZVS Buck Regulator Removes Barriers To Increased Power Throughput In Wide Input Range Point-Of-Load Applications

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## Introduction

The need for higher power density in today's electronic systems combined with higher overall efficiency has driven many changes in the Non-isolated Point-of-Load Regulator (niPOL). In an effort to improve overall system efficiency, designers are opting to avoid multiple conversion stages to get to the regulated point-of-load voltage they need. This means that the niPOL is operated at higher input voltages with higher conversion ratios than ever before. Despite this fact, the niPOL is expected to maintain the highest efficiency and still continue to shrink the total size of the power solution. There is also the added expectation that with all other performance increases that power demand from the niPOL also further increases.

The power industry has responded to this challenge by introducing many technological upgrades to the niPOL. Over the past few years, the industry has seen significant improvements in device packaging, silicon integration and MOSFET technology, yielding highly integrated, compact solutions. While these solutions work well over a narrow voltage range, the efficiency and throughput power tend to drop slightly at modest step-down ratios of 10:1 or 12:1 and fall off dramatically when they are subjected to a wide input range that can be higher, with a step-ratio approaching 36:1.

Of all the changes applied to the niPOL in the past few years, the least amount of change has been the power train topology itself. Clearly, we have seen countless control topologies like current-mode control, simulated current-mode control, digital control, etc. and power train improvements like synchronous rectification and adaptive drivers. These technologies have resulted in either incremental improvements and/or additional design complexities.

The hard switched buck regulator topology itself greatly limits improvements in the power density and throughput in a wide dynamic operating range. In order to reduce the size of a power system, you must reduce the size of its critical components. The best way to achieve this is to increase the switching frequency. Therein lies the difficulty. Increasing the switching frequency with a hard switched topology is like increasing the size of a leaky dam. There are basically three fundamental challenges:

**1. Hard Switching:** The simultaneous conduction of high current while there is high voltage imposed upon the main high-side switch causes frequency and voltage dependent switching losses and is a direct barrier to operating over a wide dynamic range. The next generation MOSFET technology with better Figures of Merit (FOM) for switching speed should allow faster switching. Fast switching has its own set of problems; hard switching (even fast switching) usually results in switch mode spiking and ringing, as well as EMI and gate driver corruption that must be dealt with. These problems are magnified at higher input voltage and frequency, making faster switching less attractive over a wider operational range requiring higher voltage or frequency.

**2. Body Diode Conduction:** The conduction of the synchronous switch-body diode is detrimental to high efficiency is detrimental to high efficiency and limits how high the switching frequency can be. The synchronous switch-body diode usually has some conduction time before the high-side switch turns on and also after the synchronous MOSFET turns off.

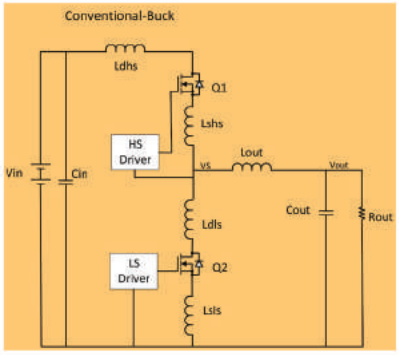
**3. Gate Drive Loss:** Switching the MOSFETs at high frequency causes higher gate drive losses.

This paper will illustrate the challenges of hard switching in a moderate and high switching frequency environment by comparing simulation models of two designs using the conventional buck regulator topology. A new buck regulator topology called "ZVS Buck" will be introduced and its integration into the Picor® Cool-Power® ZVS Buck product family will be explained. A simulation model of the new ZVS Buck regulator will show how its novel Zero-Voltage-Switching topology achieves very high-power density, efficiency, throughput power capability and wide dynamic range by reducing the effects of these three operational challenges. The ZVS Buck topology's many benefits will be described along with the theory of operation.

## Simulation Model

Figure 1 shows a typical Conventional Buck Topology diagram and the associated parasitic inductances that may be present as either the MOSFET parasitic inductances and/or the lumped parasitic inductance of the PCB traces themselves. In order to graphically show the limiting factors of this topology when used in higher frequency applications, a simulation model was constructed using best-in-class MOSFET's (and the manufacturer's SPICE models).

Figure 1.
Conventional buck topology

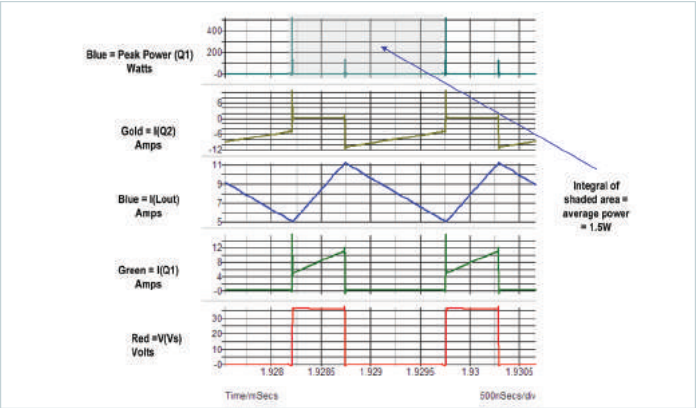



The converter design is assumed to be operating from 36 V input and stepping down to 12 V with a full load current of 8 A. The simulations were run at 650 kHz using a 2 µH inductor and 1.3 MHz using a 1 µH inductor. The MOSFET on resistance was 10 mOhms. The four parasitic inductances were set to 300 pH for Lshs and 100 pH for the other inductance values. Parasitic values are based on the available packaging technology and layout techniques associated with a Power-System-in-Package (PSiP) power design concept. The gate driver used 4 Ohm source resistance to minimize ringing and 1 Ohm sink resistance for the high-side driver for faster turn-off and 1 Ohm source and sink resistances for the low-side driver in both cases.

## Hard Switching

Figure 2 shows the simulation results of the instantaneous power dissipation in the high-side MOSFET Q1 versus the $V_S$ node voltage and current waveforms for Q1 (Green), Q2 (Red) and the output inductor Lout (Blue).

Figure 2.
650 kHz simulation 500 ns/div



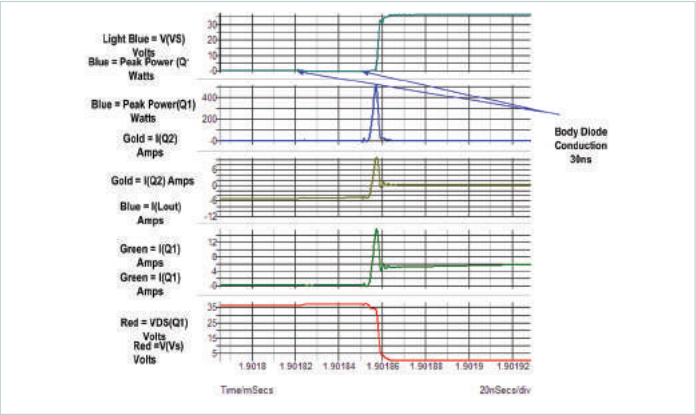

The simulation results reveal that there are very high losses at turn-on and somewhat lower losses at turn-off. The area in between are the MOSFET $R_{DS(on)}$ dominated losses, which are quite low. Dramatically improved MOSFET $R_{DS(on)}$ has occurred over the past few years. In most current designs, the conduction loss is low and more easily managed. When the instantaneous power was integrated over the switching cycle, it was found that the average power dissipation of the high-side MOSFET at 650 kHz was 1.5 W, with 0.24 W conduction, 0.213 W turn-off and 1.047 W occurring at turn-on. The primary contributor to the total loss is Q1 turn-on.

Figure 3 is a snapshot of the area just prior to and including the leading edge of the turn of the high-side MOSFET Q1. There is a 30 ns dead time between the low-side MOSFET Q2, turning off and the turn-on of Q1. This dead time is meant to ensure that cross conduction of the MOSFETs does not happen at turn-on. As a result, the body diode must commutate the current freewheeling through the output inductor. The body diode of Q2 is forward biased during this time and charge is stored in the PN junction of the diode. This charge must be swept away before the diode can block reverse voltage. This process is known as reverse recovery.

In Figure 3, the drain to source voltage of Q1 is very high; near $V_{IN}$, (influenced by the parasitic inductance of the layout) while there is very high current flowing into the body diode of Q2. The peak power is very high as Q1 must burn the reverse recovery charge of the Q2 body diode while at the same time exposed to nearly the full input voltage. The inductance in the source of the high-side MOSFET, Lshs, does not help this situation very much. At turn-on, this inductance takes away gate drive from the MOSFET due to the reverse recovery current voltage drop across it. This voltage drop is in the wrong direction, pushing the source voltage up with respect to the gate while the driver is struggling to overcome the Miller effect of turn-on. This results in a longer period of time in the Miller region and higher power dissipation in the high-side MOSFET and driver. As a result, the MOSFET can not enter the low resistance region until the Q2 body diode has recovered and can block voltage. During the recombination time after the peak recovery current has reached its maximum value, power is burned in the body diode of Q2 since it is exposed to simultaneous reverse current and reverse voltage. The power dissipation ends in the body diode after recombination is completed.

Figure 3.

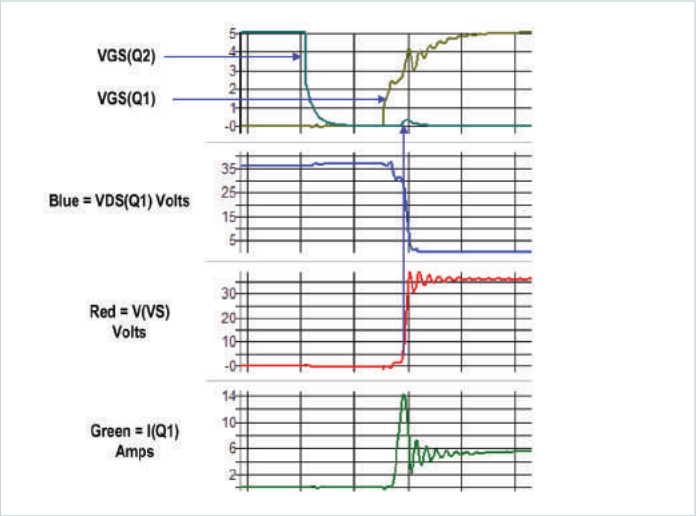
650kHz simulation 20 ns/div reverse recovery effect




The power dissipation can be slightly reduced in the high-side MOSFET by speeding up its gate drive. However, speeding up the gate drive so that Q1 will traverse the linear region more quickly will result in faster reverse recovery of the body diode of Q2 by injecting a higher reverse recovery current. The result will be a faster rising $V_S$ node due to the stored energy in the parasitic inductances. Figure 4 shows the gate drive of our 650 kHz simulation and the effect of Lshs on the drive of Q1 if it were increased 200 pH to 500 pH. Note that a bump shows up on Q2 during the rising of $V_S$. This bump is coupled to the gate driver of Q2 due to the Miller capacitance of Q2 and the dv/dt of the $V_S$ node. It is not difficult to imagine the effect of speeding up the drive to Q1. A faster dv/dt will cause a bigger bump on the gate of Q2 and more ringing. If Q2 is a low voltage device with low gate threshold, Q2 may be gated on and cause a periodic cross conduction. This cross conduction may or may not be destructive, but lower efficiency definitely will result. Higher energy stored in the parasitic inductance may also cause excessive voltage on the MOSFETs and may even require dissipative snubbing.

Figure 4.

650 kHz simulation 20 ns/div gate drive effect of increasing Lshs to 500 pH




## Higher Frequency Operation

The conventional buck simulation model was next operated with a smaller output inductor and at twice the switching frequency to keep the peak currents about the same. No other changes were made to the model. At 1.3 MHz, the total simulated losses in the high-side MOSFET increased to 2.73 W, As expected, the turn-on and turn-off losses doubled as compared to the 650 kHz simulation. The RMS switch current in Q1 remained the same so the conduction losses did not change significantly.

Considering just the losses in Q1 alone, doubling the switching frequency will result in an efficiency drop of 1.2 % minimum. The impact on efficiency would be significantly greater if the conversion ratio was higher. These results indicate that this is not the best method for size reduction and increased power throughput. To reduce the size of a power solution and still produce meaningful output power capability, the switching losses need to be addressed, enabling increased switching frequency.

## ZVS Topology

Figure 5 shows the schematic diagram for the ZVS Buck Topology. Schematically, it is identical to the conventional buck regulators except for an added clamp switch that connects across the output inductor. The clamp switch is added to allow energy stored in the output inductor to be used to implement Zero Voltage Switching.

**Figure 5.**
ZVS Buck topology

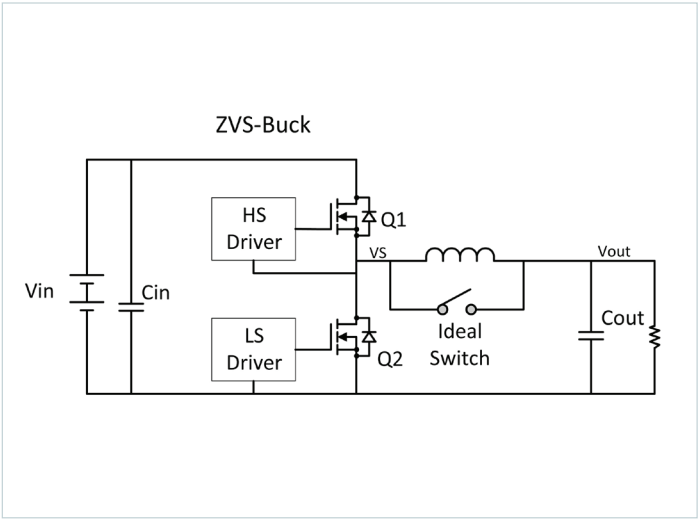
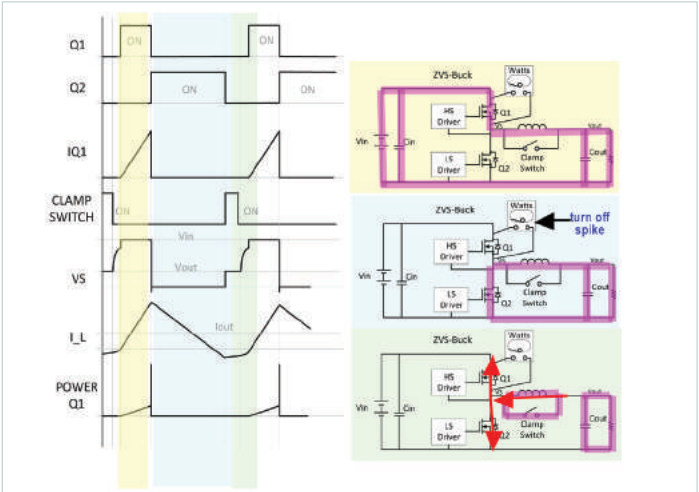



**Figure 6.**
ZVS buck timing diagram



The ZVS Buck Topology consists of basically three main states. They are defined as Q1 on phase, Q2 on phase and clamp phase. In order to understand how the Zero-Voltage-Switching action occurs, you have to assume that Q1 turns on at nearly zero voltage following a resonant transition. Q1 turns on at zero current and when the D-S voltage is nearly zero. Current ramps up in the MOSFET and output inductor to a peak current determined by the on time of Q1, the voltage across the inductor and the inductor value. During the Q1 on phase, energy is stored in the output inductor and charge is supplied to the output capacitor. The area marked in yellow shows the equivalent circuit and current flow corresponding to the Q1 on phase. During the Q1 on phase, the power dissipation in Q1 is dominated by MOSFET on resistance. The switching loss is negligible.

Next, Q1 turns off rapidly followed by a very short body diode conduction time of less than 10 ns. This body diode conduction time adds negligible power dissipation. During the current commutation to the body diode, Q1 does experience turn-off losses in proportion to the peak inductor current. Next Q2 turns on and the energy stored in the output inductor is delivered to the load and output capacitor. When the inductor current reaches zero, the synchronous MOSFET Q2 is held on long enough to store some energy in the output inductor from the output capacitor. This is noted by the inductor current going slightly negative. The Q2 on phase and equivalent circuit can be seen in the blue shaded area.

Once the controller has determined that there is enough energy stored in the inductor, the synchronous MOSFET turns off and the clamp switch turns on, clamping the $V_S$ node to $V_{OUT}$ The clamp switch isolates the output inductor current from the output while circulating the stored energy as current in a nearly lossless manner. During the clamp phase time, (which is very small) the output is supplied by the output capacitor.

When the clamp phase ends, the clamp switch is opened. The energy stored in the output inductor resonates with the parallel combination of the Q1 and Q2 output capacitances, causing the $V_S$ node to ring towards $V_{IN}$. This ring discharges the output capacitance of Q1, diminishes the Miller charge of Q1 and charges the output capacitance of Q2. This allows Q1 to turn on when the $V_S$ node is nearly equal to $V_{IN}$ and in a lossless manner. The clamp phase of operation, including the resonant transition and equivalent circuit, is shown as the green section. Here it is important to point out that when the clamp switch is on, the current circulates as shown by pink current loop and when the switch is off, the current flows as shown by the red arrows.

**This topology addresses the limitations shown previously in several important ways:**

1. As long as there is a clamp phase, there is no body diode conduction that requires high reverse recovery current prior to turning on the high-side MOSFET.
2. The turn-on losses are almost totally eliminated.
3. The high-side MOSFET gate drive is unaffected by the parasitic inductance Lshs. The Miller effect is removed from the high-side MOSFET at turn-on due to the ZVS action and lack of turn-on current slug. This allows the high-side gate driver to be smaller and consume less power. The high-side MOSFET does not have to turn on particularly fast, allowing for smooth waveforms and less noise.

## Comparison Simulation

Figure 7 shows the schematic of the ZVS Buck Topology with the previous parasitic inductance values used. A simulation was run of the same 36 V to 12 V regulator operated at 8 A at 1.3 MHz to compare the losses in the high-side MOSFET with those of the previous designs. The ZVS Buck used a 230 nH inductor and the same MOSFETs and gate driver characteristics used in the previous simulations.

Figure 7.
ZVS Buck with parasitic inductances

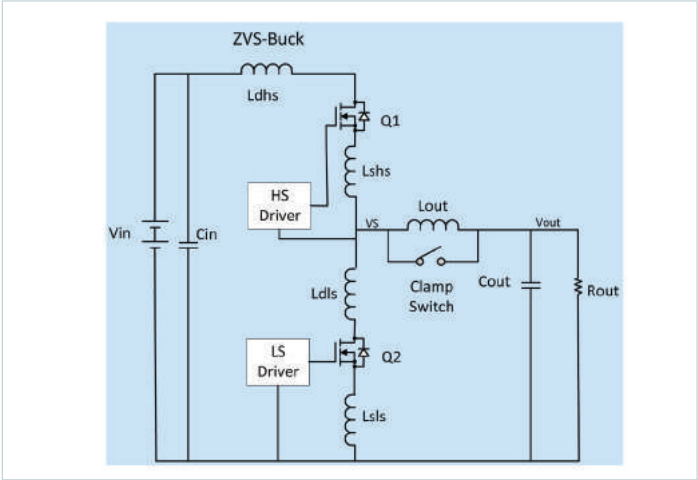



Figure 8 shows the simulation results of the ZVS Buck Topology running at 1.3 MHz and the corresponding instantaneous power curve for the high-side MOSFET, Q1. The average power dissipation including switching losses and conduction losses measured 1.33 W in the high-side MOSFET Q1, even lower than the conventional regulator operated at half the switching frequency and using a larger inductor. The savings in the high-side MOSFET power consumption when comparing the results of both design simulations at 1.3 MHz is much greater; i.e. 1.37 W. From the power curve in Figure 8, it can be seen that the turn-on losses are virtually zero and there is no high current spike in Q1 at turn-on. There is no body diode conduction prior to the turn-on of Q1 and no reverse recovery effects, including reverse recovery loss in the body diode of Q2.

The figure shows the resonant transition ZVS action consisting of the parallel combination of both MOSFET (Q1 and Q2) output capacitances ringing with Lout. It can also be seen that the turn-on of Q1 does not happen exactly at zero volts. The best overall efficiency is generally obtained by switching Q1 with some residual voltage across it to reduce the amount of stored energy requiring circulation during the clamp phase. There is a tradeoff made to minimize the losses associated with clamp phase versus the power savings by switching Q1 at exactly zero volts. The gate driver turn-on losses also benefit from the removal of the Miller charge that occurs as a result of ZVS action. The driver does not have to discharge the G-D capacitance of Q1, so the losses in the high-side driver go down. In addition, the high-side driver does not have to struggle against the parasitic inductance Lshs at turn-on since the driver supplies less charge at turn-on and there is no high current slug storing energy in Lshs.

Figure 8.

ZVS Buck simulation waveforms

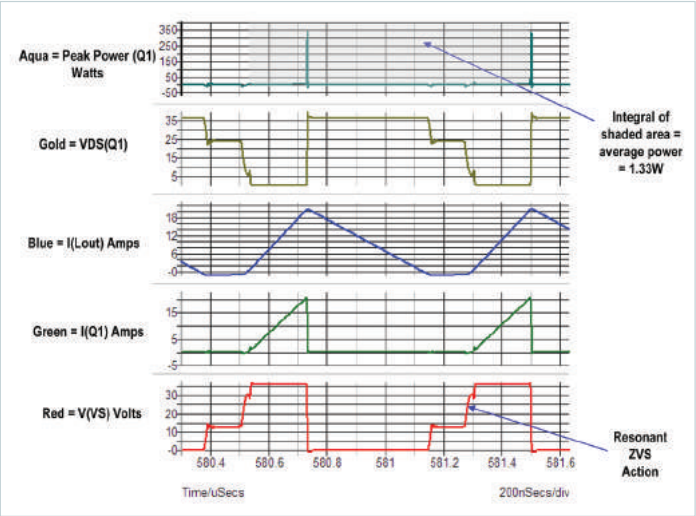
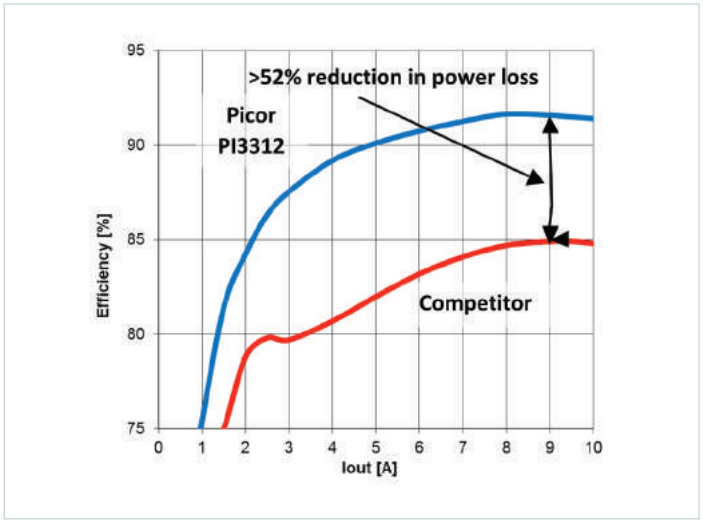



Figure 9 shows the performance difference between a current, competitive hard switched solution and the performance of the ZVS Buck Topology in a 24 $V_{IN}$ to 2.5 $V_{OUT}$ (9.6:1) 10 A design. The full load efficiency difference is nearly 6.5 %, (with a notable difference in light load efficiency as well) resulting in an improvement of greater than 52% in power loss at the measurement point of 9 A.

Figure 9.

ZVS Buck 9.6:1 step down 24 V – 2.5 V @ 10 A performance vs competitive solution



## Additional Benefits

By integrating the ZVS Buck Topology with Picor's high performance silicon controller architecture, the PI33XX family of wide input range DC-DC regulators is developed. This DC-DC solution consists of a 10 mm X 14 mm SiP containing all of the circuitry required to form a complete power system with the addition of an output inductor and a few ceramic capacitors. The high switching frequency allows the inductor to be very small and the total solution size to be smaller (25 mm X 21.5 mm) than competitive integrated solutions, while producing up to 120 W of output power with a peak efficiency of 98%. With a 20 ns minimum on time, the PI33XX can operate from 36 V input to 1 V output at 10 A load with an efficiency exceeding 86% and no reduction of output current over the range of output voltages from 1 V to 15 V.

The combination of advanced silicon and the ZVS Buck topology yields some additional benefits to wide input range and high efficiency. Since the ZVS topology is inherently stable with a control to output transfer function having a gain slope of -1 and a phase shift of 90 degrees, a very wide bandwidth feedback loop is possible, aided by high switching frequency. The PI33XX requires no external compensation (although it is possible to add some). The closed loop crossover frequency typically is 100 kHz with 55 degrees of phase margin and 20 dB of gain margin. The high closed loop gain and small output inductor allow the closed loop output impedance to be low over a wide frequency range. This results in very fast transient response, with recovery times in the 20 – 30 µs range while using modest ceramic output capacitance values and without the aid of additional bulk storage capacitors. A very accurate input feed forward method allows the error amplifier output voltage to accurately reflect the output load requirement. This allows implementation of a very simple current sharing method for connecting Si's in parallel to increase output power. Only a single connection needs to be made to each PI33XX error amplifier to share the load accurately. Additional connections can be made if the user wishes the units to track one another and be synchronized together.

The PI33XX can be synchronized with like models up to six in parallel using interleaving. The PI33XX has nearly ideal synchronous rectifier drive, allowing only single digit nanosecond body diode commutation times between turn-off of the high-side MOSFET to turn-on of the synchronous MOSFET. This helps reduce turn-off losses in the high-side MOSFET and body diode conduction losses. In addition to the high efficiency benefits at high loads, the PI33XX uses a very high efficiency biasing system and pulse skipping mode that achieves outstanding light load efficiency as well. See Figure 9.

## Flexibility

The Picor high performance silicon controller architecture utilizing zero voltage switching can be applied to other topologies like the Boost Topology and the Buck-Boost Topology and yield similar benefits just by rearranging the power switches. This will allow virtually any combination of power conversion to take place at high efficiency and even higher input voltages while incurring low switching losses, producing high throughput power and decreasing the solution size.

## Conclusion

This paper introduced and detailed the challenges that have existed up to now when attempting to operate the conventional Buck Topology at high input voltage and switching frequency. Operation of a buck converter at high frequency and input voltage is desirable to reduce the overall size of a power system solution so that it could be used to replace dual conversion stages and operate over a wider input range at high efficiency. It has been shown that in order to operate at higher switching frequencies, turn-on losses of the high-side MOSFET need to be reduced or eliminated.

ZVS Buck Topology was presented as the means to achieve the required size reduction without reducing throughput power. A new product, called the PI33XX was introduced that utilizes a Picor high performance silicon controller architecture and contains the necessary features to allow wide input range 8 V – 36 V input to various outputs such as 1 V, 2.5 V, 3.3 V, 5 V, 12 V and 15 V at high throughput power and efficiency. Finally, it was explained that the same high performance silicon controller architecture can be used to address hard switching applications that are typically done with either Boost or Buck-Boost topologies, yielding significant throughput power and density improvements.

The author is a Principal Engineer Picor semiconductor solutions, Vicor Corporation. He has more than twenty-five years experience in power systems design and is a member of the IEEE.

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